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# **ADVANCED INVESTIGATION OF A TWO-PHASE CHARGE-COUPLED DEVICE**

BY

W. F. KOSONOCKY AND J. E. CARNES

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## FOREWORD

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SUMMARY

The performance of experimental two-phase charge-coupled shift registers constructed using polysilicon gates overlapped by aluminum gates has been studied. Shift registers with 64, 128, and 500 stages have been built and operated. Devices were operated at the maximum clock frequency of 20 MHz. Loss per transfer of less than  $10^{-4}$  has been demonstrated for fat zero operation. The effect upon transfer efficiency of various structural and materials parameters has been investigated including substrate orientation, resistivity, and conductivity type; channel width and channel length; and method of channel confinement. Operation of the devices with and without fat zero has been studied as well as operation in the complete charge-transfer mode and the bias charge, or bucket-brigade mode. The analytical section of the report contains a brief review of the free-charge-transfer characteristics of CCD's and a discussion of interface state trapping effects including a quantitative expression for the loss due to the trapping along the channel edge. The theoretical models have been verified by the operation of experimental devices.

## I. INTRODUCTION

Charge-coupled semiconductor devices (ref. 1) consist of closely spaced MOS capacitors that are pulsed into deep depletion by the clock-phase voltages. For times much shorter than that required to form an inversion layer of minority carriers by thermal generation, potential wells are formed at the silicon surface. These potential wells can be used to store and transport minority carriers representing information. The signal charge can be introduced either electrically or optically. The propagation of the information is accomplished by clock pulses applied to the electrodes of the successive MOS capacitors (i.e., charge-coupled elements), resulting in a motion or spilling of charges from shallow potential wells to deeper potential wells. Such propagation of signal into the successive minima of the surface potential produces a shift register for analog signals that has a signal transfer efficiency approaching unity. Such analog shift registers may be used for various signal-processing applications such as electronically variable delay lines or self-scanning photosensor arrays. Charge-coupled shift registers for digital signals can also be constructed, and by adding simple charge-refreshing stages (refs. 2,3), digital memory is possible.

If the charge-coupled structures are formed with symmetrical potential wells, at least three clock phases are required to determine the directionality of the signal flow. Two-phase operation requires that the charge-coupled structures be formed so that the potential wells induced by the phase-voltage pulses are deeper in the direction of the signal flow. In this case, as one phase voltage is lowered, the resulting potential barriers force a unidirectional signal flow.

The first charge-coupled devices (CCD's) were made by the thick-oxide PMOS process (refs. 2-5). The major limitation of this process is the etching of the separation between the gates, which should be no larger than about 0.1 mil ( $\sim 2.5 \mu\text{m}$ ) in order to control the surface potential in the resulting gap.

The sealed-channel polysilicon-aluminum structures described in this report are the most compact structures that can be fabricated with more or less conventional layout rules. The self-aligning gate construction of these devices allows fabrication of charge-coupled structures with gate separation comparable to the thickness of the channel oxides, as well as having the channel oxide always covered by one of the metallizations. The important advantage of the silicon-gate process is that it provides a very simple method for the construction of two-phase CCD's. The two-phase CCD's described in this report employ two thicknesses of channel oxide for the formation of the asymmetrical potential wells needed for the unidirectional flow of signal.

The objectives of the work described in this report were twofold. First, using 64- and 128-stage two-phase devices initially developed under a previous NASA contract (NAS1-10983 with Final Report NASA CR-21486) as test vehicles, determine the effect of process variations, substrate orientation, conductivity type, and method of channel confinement upon device efficiency and the effect of substrate resistivity upon device speed. Secondly, using the results of the first objective, design and fabricate a 500-stage two-phase shift register using the polysilicon-aluminum technology.

In Section II of this report the theory of free-charge transfer and interface-stage trapping in CCD's is reviewed to provide a basis for discussion and analysis of the experimental results. Section III provides details of experimental device fabrication, structure, and packaging of both the 64- and 128-stage devices and the new 500-stage device. The experimental results are reported in Section IV and discussed and correlated with the theory in Section V. Finally, conclusions are presented in Section VI.



## II. CHARGE-TRANSFER ANALYSIS

### A. Free-Charge Transfer

1. Introduction. - The utility of CCD's for various applications depends to a great extent upon the two interrelated questions of how fast and how completely charge can be transferred between adjacent potential wells. When interface-state trapping is ignored, the answers to both of these questions are known if one knows how much charge remains in the transferring potential well as a function of time. An outline of the free-charge transfer analysis that yields such information is given in this section; a more detailed discussion can be found in References 6 and 7. While the discussion assumes a three-phase device, the results are valid for any single transfer regardless of the number of phases.

There are three separate, conceptually identifiable mechanisms, or "driving forces" that cause charge to move from one potential well to an adjacent one of lower energy (see Fig. 1). The first is thermal diffusion due to the random thermal motion of the carriers that causes charge to move from regions of higher concentration to regions of lower concentration. The second mechanism is due to the repulsion of the like-charged carriers that make up the signal and is referred to as "self-induced drift." It is basically a drift mechanism in which the electric field is produced by the charge carriers themselves. The third mechanism is referred to as "fringing-field drift." Here, the electric field arises from the externally applied clock voltages. In the following discussion it will be shown that fringing-field drift may appreciably speed up the charge-transfer process, and appropriately designed CCD structures can result in highly efficient transfer ( $\eta = 99.99\%$ ) at 10-MHz-bit rates (neglecting interface-state trapping).

2. Thermal Diffusion. - Strictly speaking, the time decay of charge remaining in the transferring potential well due to thermal diffusion alone depends upon the initial-charge-concentration profile. However, a Fourier analysis of the problem indicates that the decay approaches an exponential profile for long times with a decay constant  $\tau_{th}$  given by

$$\tau_{th} = L^2/2.5D \quad (1)$$

where  $L$  is the center-to-center electrode spacing and  $D$  is the diffusion constant. In this problem it is assumed that a potential barrier prevents charge motion in the reverse direction while the receiving potential well serves as a perfect sink for carriers in the forward direction.

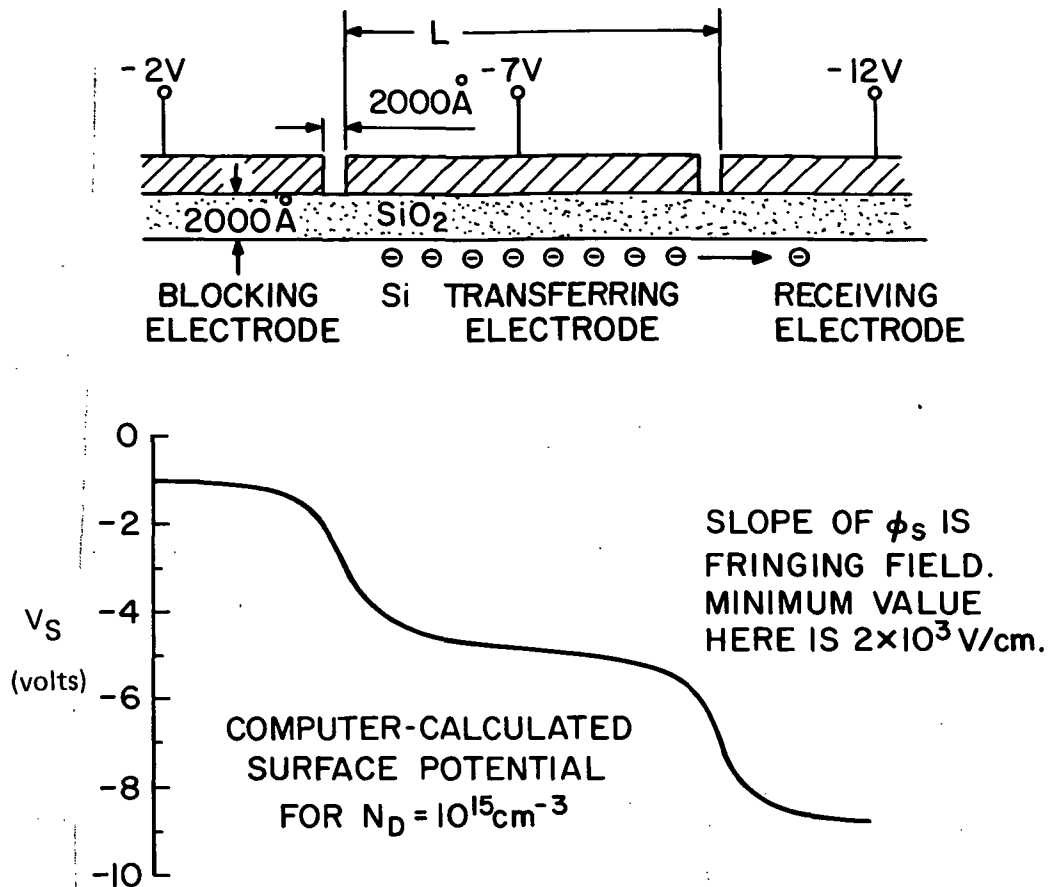


Figure 1. Cross section of three-phase CCD. Charge transfers from under center electrode to the right. The surface potential in the absence of signal charge as calculated by computer is shown in the lower half of the figure.

Thus, if the carriers were not charged and thermal diffusion were the only transfer mechanism, the total number of carriers remaining in the transferring well as a function of time  $N_{\text{tot}}(t)$  would be given by

$$N_{\text{tot}}(t) = N_{\text{tot}}(0) \exp \left( -\left( \frac{2.5D}{L^2} \right) t \right) \quad (2)$$

3. Self-Induced Drift. - The drift of the carriers under the influence of the electric field produced by the signal charge itself is an important effect at carrier concentration levels above  $\sim 10^{10} \text{ cm}^{-2}$ .

There are at least two different methods of approaching this problem: the gradient method and the integral method (see ref. 6). Both lead to the same conclusion, i.e., the charge remaining decays hyperbolically in time according to the following equation

$$N_{\text{tot}}(t) = N_{\text{tot}}(0) \frac{t_0}{t + t_0} \quad (3)$$

where

$$t_0 \approx \frac{L^2 C_{\text{ox}}}{1.57 \mu q n_0} \quad (4)$$

and

$C_{\text{ox}}$  is the oxide capacitance per unit area ( $\text{F}/\text{cm}^2$ )  
 $\mu$  is the field-effect mobility ( $\text{cm}^2/(\text{V} \cdot \text{sec})$ )  
 $q$  is the electronic charge (C)  
 $n_0$  is the initial uniform carrier concentration ( $\text{cm}^{-2}$ )

A hyperbolic time decay is very fast for short times ( $t \leq 100 t_0$ ), but becomes comparatively slow for long times. It can be shown that after  $t = 1.6 \tau_{\text{th}}$ , the decay due to thermal diffusion proceeds faster than that caused by self-induced drift. Thus, self-induced drift is a very fast process effective in transferring the first 90 to 99% of charge. It becomes ineffective, however, in attaining transfer efficiencies of 99.99%.

4. Fringing-Field Drift. - A third mechanism that can have a dominant effect on charge transfer, especially at low signal charge concentration levels, is fringing-field drift. The fringing fields referred to are the electric fields at the Si-SiO<sub>2</sub> interface along the direction of charge transfer that arise from the externally applied clock voltages. In other words, the fringing field at any point along the interface is the slope of the surface potential at that point (see Fig. 1).

Fringing-field magnitudes have been calculated by an approximate analysis and computed numerically for the case of closely spaced electrodes (ref. 8). They depend upon the electrode length, the clock-voltage magnitude, the oxide thickness, and the substrate-doping density.

The minimum value of the fringing field occurs at the center of the transferring electrode and can be approximated by the following expression

$$E_{\text{FMIN}} = 6.5 \frac{X_{\text{ox}}}{L} \frac{V}{L} \left( \frac{5X_d/L}{5X_d/L + 1} \right)^4 \quad (5)$$

where  $X_{\text{ox}}$  is oxide thickness,  $V$  is one-half of the total clock-pulse voltage,  $L$  is the gate length, and  $X_d$  is the depletion depth at the center of the transferring electrode. For the closely spaced electrode structures studied, it was found that the average fringing-field magnitude is twice the minimum value, so that the time required for a single carrier to transit across the length of the transferring gate, i.e., the signal carrier transit time,  $\tau_t$ , is given by

$$\tau_t = \frac{L}{2\mu E_{\text{FMIN}}} = \frac{L^3}{13 \mu X_{\text{ox}} V} \left( \frac{5X_d/L + 1}{5X_d/L} \right)^4 \quad (6)$$

However, our computer studies have shown that it takes longer than one  $\tau_t$  to remove all of the charge from the transferring gate. Because of the combined effects of the nonuniform fringing field and the thermal diffusion that tends to oppose charge transfer, the total remaining charge decays exponentially in time with the final decay constant  $\tau_f$ . Furthermore, it was found for the closely spaced gate structures studied that  $\tau_f$  was equal to one-third  $\tau_t$ , and since an analytical expression is available for  $\tau_t$  [Eq. (6)] the decay rate due to fringing-field drift can be calculated

$$N_{\text{tot}}(t) = N_{\text{tot}}(0) \exp \left( -\frac{3t}{\tau_t} \right) \quad (7)$$

For doping densities lower than  $\sim 10^{15} \text{ cm}^{-3}$  and gate lengths less than 1 mil (25  $\mu\text{m}$ ), the fringing-field drift mechanism significantly speeds up the transfer of the last few percent of charge.

## B. Trapping Effects In Fast Interface States

Fast interface states (FIS) exist in the silicon forbidden gap at the silicon-insulator interface and can exchange charge with the silicon conduction and valence bands. When a charge carrier is in one of these states it is localized and cannot move. They are caused by the abrupt

termination of the silicon lattice periodicity, but can also result from chemical impurities, work damage, and stresses induced by thermal-expansion mismatch between the insulator and silicon. Fast states are characterized by their area-density per unit-energy interval,  $N_{SS}(\epsilon)$ , which may vary as a function of energy, and by their capture cross section for electrons and holes,  $\sigma_n$  and  $\sigma_p$ , in  $\text{cm}^2$ . Many factors are known to affect  $N_{SS}$  for the Si-SiO<sub>2</sub> interface, including oxide-growth conditions, silicon orientation, and annealing procedures (refs. 9,10). Generally, the density is a minimum near the center of the gap and gradually increases to peaks about 0.1 eV above and below the two bands (ref. 11). The (111) silicon surface orientation results in about one order of magnitude more fast states than the (100) orientation (ref. 12), while steam-grown oxides have lower fast-state densities than dry oxides (ref. 11). A 500°C heat-treatment step in hydrogen gas after aluminum deposition reduces fast-state densities to the  $10^{10}(\text{cm}^2 \cdot \text{eV})^{-1}$  level (ref. 13). Capture cross sections for electrons have been measured to be between  $10^{-15}$  and  $10^{-16} \text{cm}^2$ , and  $\sigma_p$  values range between 2 and  $4 \times 10^{-17} \text{cm}^2$  (ref. 11).

A straightforward model of interface state trapping successfully predicts many features of CCD loss behavior. The model that has been assumed consists of a uniform (or slowly varying) density in energy of interface states, denoted  $N_{SS}$ , which exist at the Si-SiO<sub>2</sub> interface. These states will trap free electrons or holes at a rate proportional to the number of free electrons or holes and the number of empty or filled states, respectively. The states will emit or de-trap electrons or holes at a rate proportional to the number of filled or empty states, respectively, and the Boltzmann factor appropriate for the energy of the states (ref. 9). Thus, the rate of change of occupation of the fast states at any given energy level  $\epsilon$  below the conduction band is given by

$$\begin{aligned} \frac{dn_{ss}}{dt} = & k_1 (N_{SS} - n_{ss})n_s - k_2 n_{ss} e^{-\epsilon/kT} \\ & - k_3 n_{ss} p_s + k_4 (N_{SS} - n_{ss}) e^{-(\epsilon_g - \epsilon)/dT} \end{aligned} \quad (8)$$

where  $n_{ss}$  is the number of occupied states in  $(\text{cm}^2 \cdot \text{eV})^{-1}$   
 $N_{SS}$  is the interface-state density in  $(\text{cm}^2 \cdot \text{eV})^{-1}$   
 $n_s$  is the density of free electrons at the surface in  $\text{cm}^{-2}$   
 $\epsilon$  is the energy of the states below the conduction band edge  
 $\epsilon_g$  is the energy width of the forbidden gap  
 $k$  is Boltzmann's constant  
 $T$  is absolute temperature  
 $k_1, k_2, k_3$ , and  $k_4$  are constants

In principle, if we know how  $n_s$  varies with time, then by using Eq. (8) we can solve for  $n_{ss}$  as a function of time and energy. By integrating over energy, we find the total amount of trapped charge as a function of time. By comparing the total number trapped at the beginning of the transfer-in period with that trapped at the end of the transfer-out period we can obtain the total number of carriers lost into interface states for each transfer. This procedure can be used to calculate the interface state loss vs. CCD clock frequency.

When the surface potential is large enough so that a negligible number of majority carriers exist at the interface, by using Eq. (8) it can be shown that even though thermal equilibrium does not apply, it is appropriate to define a quasi-Fermi level,  $E_Q$ , which simultaneously describes the occupation of the fast states and the density of minority carriers at the interface;  $E_Q$  is given by

$$E_Q = kT \ln \frac{k_2}{k_1 n_s} \quad (9)$$

Using Eq. (8), we can also show that if  $n_s$  is abruptly changed, the fast states will approach the new occupation levels with the following time constants

$$\tau_{\text{fill}} = \frac{1}{k_1 n_s} \quad (10)$$

$$\tau_{\text{empty}} = \frac{1}{k_2} e^{\epsilon/kT} \quad (11)$$

Thus, it turns out that many of the fast states, especially those located further from the band edge ( $\epsilon$  greater), can fill faster than they can empty and will, therefore, remove charge from the signal packet that is propagating through the CCD.

By making certain simplifying assumptions, one can arrive at a simple expression for the number of carriers lost into fast states at each transfer. The necessary assumptions are:

- (1) A charge  $n_{s,0}$  is always present in the potential well. This establishes the occupation level before the signal arrives.
- (2) The signal charge is transferred into the well instantaneously at  $t = 0$  and is transferred out of the well instantaneously at  $t = (1/2f)$  (two-phase operation).

- (3) The magnitude of the signal is large enough to cause nearly all of the interface states to fill instantaneously.
- (4) The quasi-Fermi levels define sharp cut-offs in occupation, i.e., all states above  $E_Q$  are empty, all states below are full.

With these assumptions and  $N_{SS}$  assumed constant in energy, we can write the number of carriers lost into fast states per transfer per  $\text{cm}^2$  as

$$N_{\text{LOSS}} = N_{SS} \left[ kT \ln(k_2/2f) - kT \ln(k_2/k_1 n_{s,o}) \right] \quad (12)$$

$$N_{\text{LOSS}} = kT N_{SS} \ln \left( \frac{2f}{k_1 n_{s,o}} \right)$$

Figure 2 schematically follows the derivation of Eq. (12).

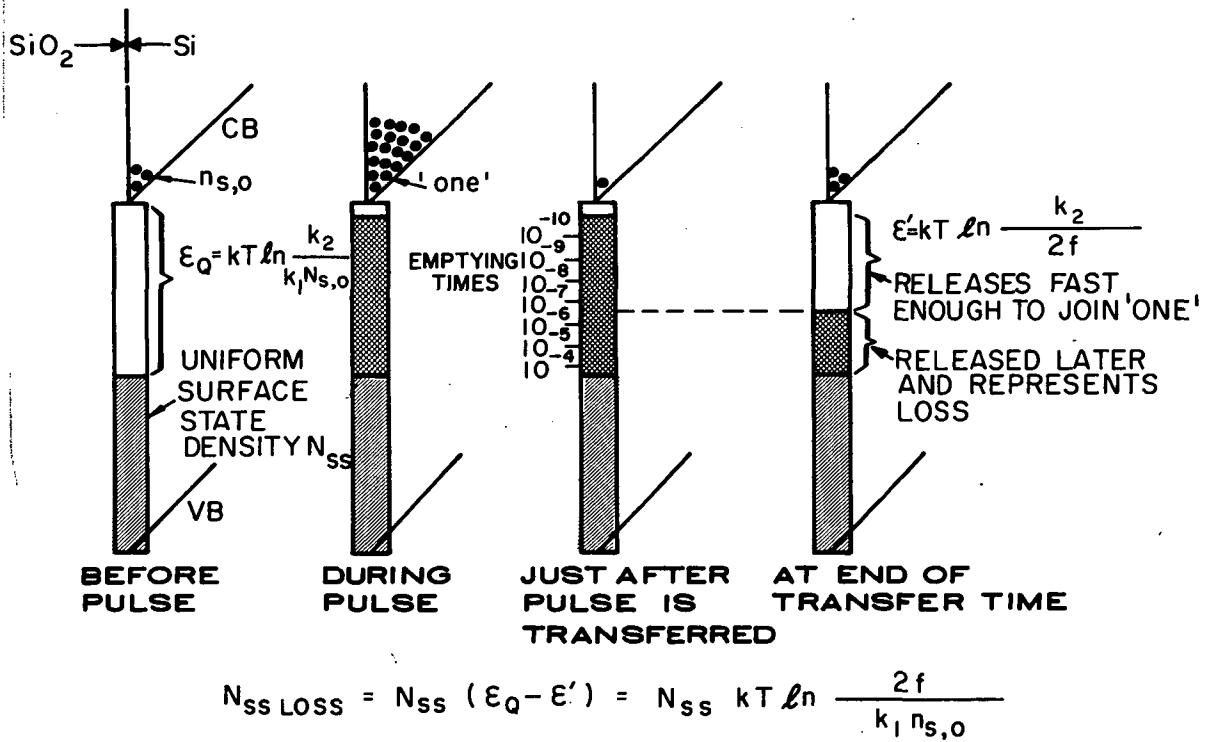


Figure 2. Schematic representation of the "before-after" interface state model.

This equation points out the linear dependence of loss upon interface state density, the  $\ln f$  frequency dependence, and the  $\ln(1/n_{s,o})$  background-charge dependence. Thus, when  $n_{s,o}$ , the fat zero, is increased, fast-state losses decrease.

Equation (12) is not exact because of the simplifying assumptions that were made. When these assumptions are removed (item (2) on p. 9 excepted), an integral expression for  $N_{LOSS}$  can be written, and a fit to computer solutions indicates that a general expression for fast-state losses can be written as follows

$$N_{LOSS} = \left( \frac{n_s/n_{s,o}}{n_s/n_{s,o} + 1} \right) kTN_{SS} \ln \left( 1 + \frac{f}{k_1 n_{s,o}} \right) \quad (13)$$

Equation (13) is similar to Eq. (12) except the prefactor indicates that when the signal level approaches zero the loss also approaches zero, as we intuitively know it must. Another difference is the additional term in the  $\ln$  argument. This has the effect of making  $N_{LOSS}$  proportional to  $f/k_1 n_{s,o}$  when  $f/k_1 n_{s,o} \ll 1$ .

### C. The Edge Effect

The discussion of fast-state losses in the preceding section has assumed a potential well with steep walls so that the background charge or fat zero is spread uniformly in all regions and is present at every point where signal charge, when present, resides. However, actual potential wells have sloping sides, and there is a region along the edges that does not benefit from the presence of fat zero as shown in Fig. 3.

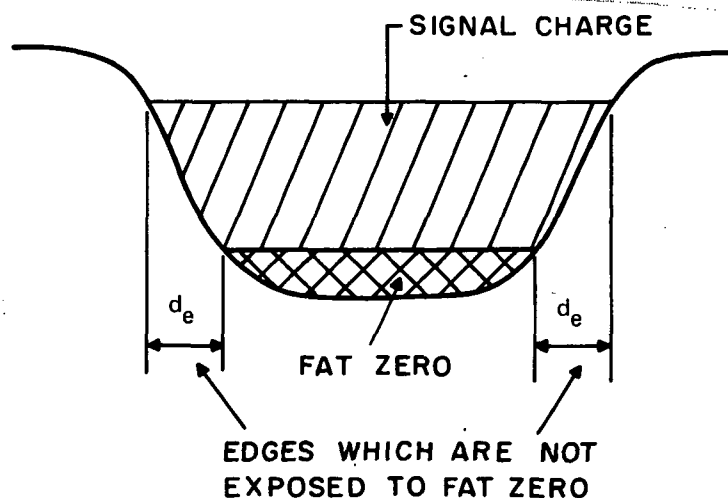


Figure 3. Cross section across a CCD channel showing the rounded potential well and the edge areas that are never exposed to fat zero.



In this edge region the conduction-band charge is very low and the quasi-Fermi level tends toward the center of the gap. In this case, the simplified theory predicts a loss per transfer given by

$$N_{\text{LOSS}} = N_{\text{SS}} \left( \frac{E_g}{2} - kT \ln \frac{k_2}{2f} \right) \quad (14)$$

The extent of the edge region will depend mainly upon the doping density of the substrate. Assuming a simple one-dimensional, uniform-space-charge case, it can be shown, using the one-dimensional Poisson equation, that the potential changes from 20% to 80% of the total well depth,  $V_{\text{well}}$ , in a distance  $d_e$  given by

$$d_e = \sqrt{\frac{\epsilon_s V_{\text{well}}}{2q N_D}} \quad (15)$$

The relative importance of the losses in the edge region depends upon the geometrical factors involved - the relative amount of edge region compared with the total area. There is also the question of whether the edges perpendicular to the channel should be treated in the same manner as the edges parallel to the channel. Since the transverse edges are subjected to the transferring fat zero once each period, it is expected that the fast states there will remain occupied, and the losses into these edges should be relatively unimportant compared with the parallel edges that never "see" fat zero.

For the case of an 80% full well signal, one can write the fractional loss per transfer into the parallel edges,  $\epsilon_{s, \text{parallel}}$ , according to:

$$\epsilon_{s, \text{parallel}} = \frac{2d_e L N_{\text{LOSS}}}{LW N_{\text{SIG}}} = \frac{2qd_e L N_{\text{SS}} \left( \frac{E_g}{2} - kT \ln \frac{k_2}{2f} \right)}{0.8 V_{\text{well}} C_{\text{ox}} LW} \quad (16)$$

where

- $N_{\text{LOSS}}$  is the number per  $\text{cm}^2$  lost into fast interface states along the edges
- $N_{\text{SIG}}$  is the number of signal carriers per  $\text{cm}^2$
- $L$  is the length of the gate parallel to the channel
- $T$  is the temperature ( $= 300^\circ\text{K}$ )
- $W$  is the width of the channel
- $C_{\text{ox}}$  is the oxide capacitance per unit area ( $= 1000 \text{ \AA}$ )

Using Eq. (15) for  $d_e$  and typical values ( $V_{well} = 4$  V and  $f = 1$  MHz), Eq. (16) can be written

$$\epsilon_{s, \text{ parallel}} = 3.9 \times 10^{-4} \left( \frac{1}{w_{\text{mils}}} \right) \left( \frac{N_{ss}}{10^{10}} \right) \left( \frac{10^{15}}{N_D} \right)^{1/2} \quad (17)$$

Figure 4 is a plot of Eq. (17) assuming  $N_{ss} = 2 \times 10^{10}$  for several different values of doping density.

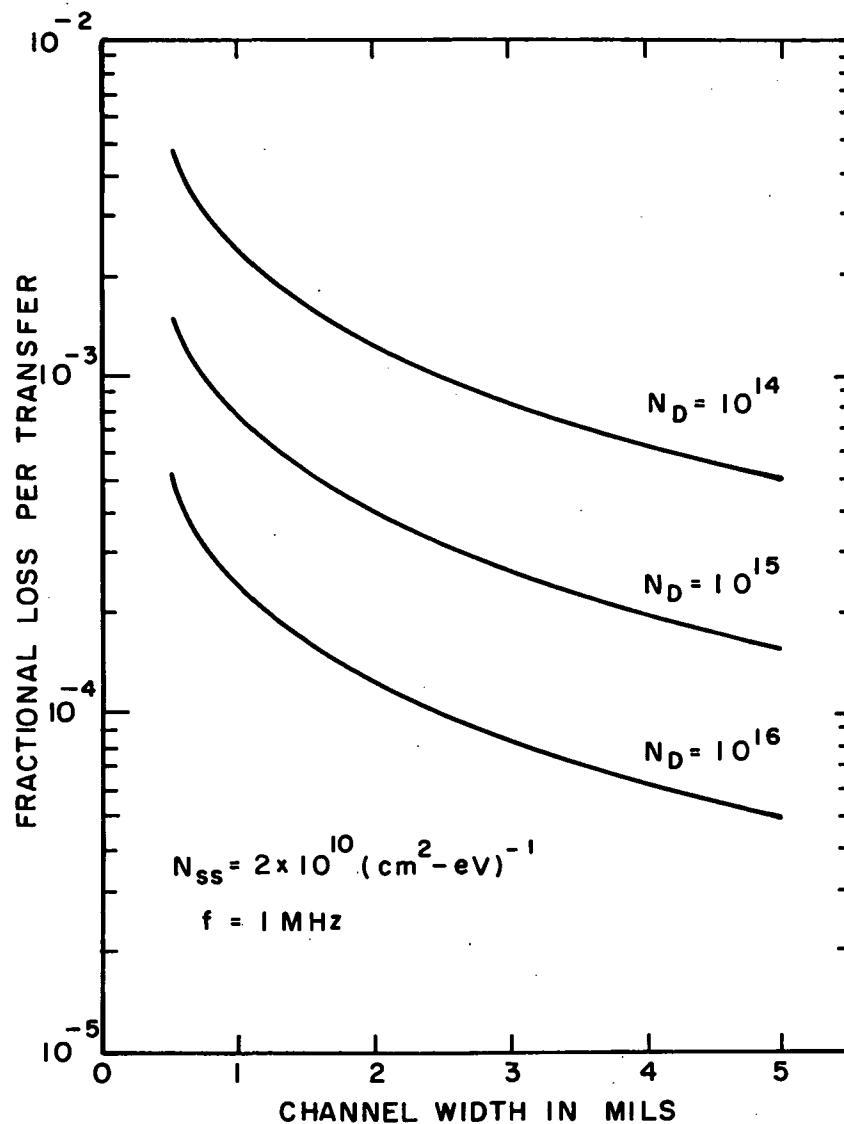


Figure 4. Fractional loss per transfer vs. channel width for various substrate doping levels as predicted by the edge-effect trapping model.

#### D. Channel Confinement

In CCD operation the signal charge must be confined to a narrow potential well called the channel. This channel should provide a deep and abrupt potential well where the surface potential changes in response to the clock pulse voltages. The region outside of the channel, the field region, should be insensitive to clock voltage changes and should be in accumulation.

There are three general methods for channel confinement:

- (1) two thicknesses of oxide or thick-field oxide,
- (2) guard-ring diffusion or "channel stops," and
- (3) electrostatic guard rings in the form of polysilicon layers (ref. 14).

Computer analyses of the channel-confinement problem using channel stop diffusions and two thicknesses of oxide have been made\*, and typical results for two thicknesses of oxide are shown in Fig. 5. The surface potential cross section is shown for several different substrate

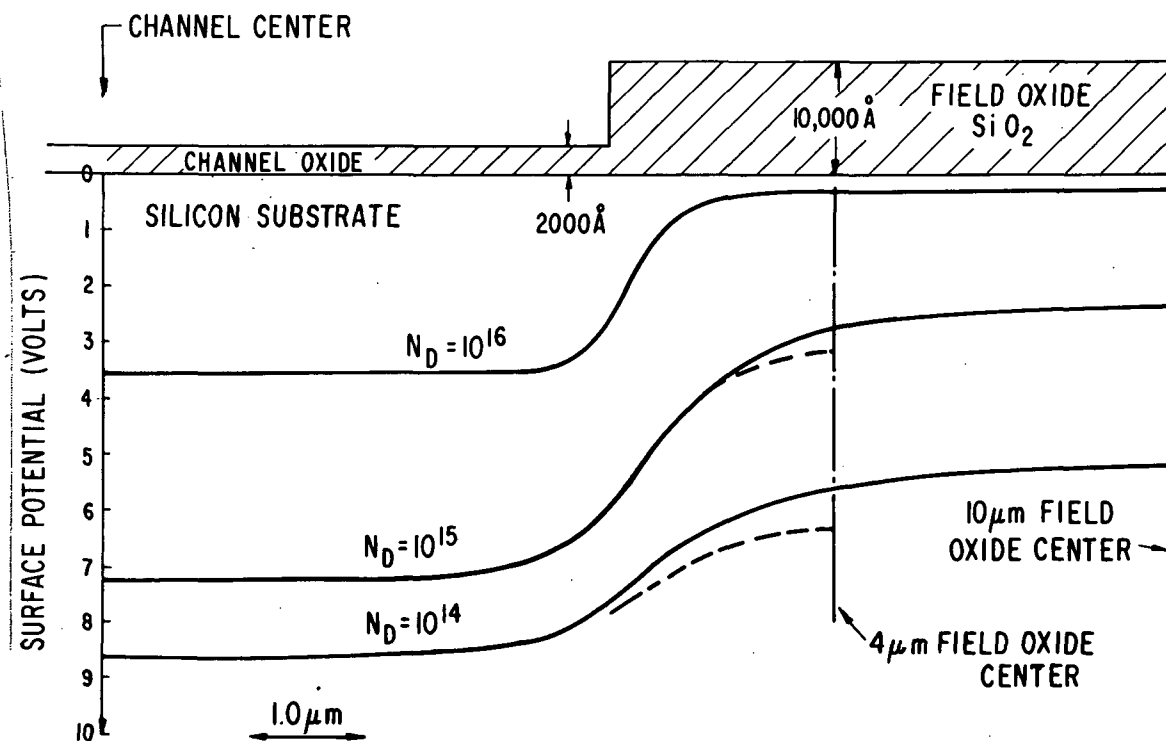


Figure 5. Computer-generated surface-potential profiles for thick-oxide channel confinement.

\*These computer studies were performed by Lish-Yann Chen.

CHANNEL CENTER

CHANNEL STOP DIFFUSION

$\text{SiO}_2$

2000 Å CHANNEL OXIDE

SURFACE POTENTIAL (VOLTS)

0

1

2

3

4

5

6

7

8

9

10

1.0  $\mu\text{m}$

SUBSTRATE DOPING  
 $N = 10^{14} \text{ cm}^{-3}$

CLOCK VOLTAGE = 10V

CHANNEL STOP DOPING LEVEL

$N = 2.1 \times 10^{17} \text{ cm}^{-3}$

$1.8 \times 10^{17}$

$1.1 \times 10^{17}$

$5 \times 10^{16}$

$1.7 \times 10^{16}$

$4.5 \times 10^{15}$

15

Ideally, the diffusion-channel stops should be very abrupt and relatively low doped ( $10^{17}$  to  $10^{18}$   $\text{cm}^{-3}$ ).

The important difference between the first two methods of channel confinement and the polysilicon electrostatic guard rings, also referred to as polysilicon field shield, is that in the latter case the surface potential at the channel stop can be determined by an externally controlled potential. Thus, the regions between the CCD channels can be accumulated or held at any other surface potential.

### III. TWO-PHASE CHARGE-COUPLED SHIFT REGISTERS

#### A. Fabrication of Experimental Devices

1. The Basic Polysilicon-Aluminum Two-Phase CCD. - The charge-coupled devices initially described by Boyle and Smith (ref. 1) require three or more phase clocks to obtain the directionality of the signal flow. However, for most applications such as self-scanning photosensor arrays or digital shift registers, high packing density and better performance may be achieved with two-phase charge-coupled structures. The asymmetrical potential wells or barriers in the surface potential, needed to provide the directionality of the information flow for the two-phase operation, can be achieved by incorporating one of the following features into the CCD structure:

- (1) two thicknesses of the channel oxide,
- (2) dc offset voltage between two adjacent gates powered by the same phase voltage,
- (3) two levels of fixed charge in the channel oxide, or
- (4) ion-implanted barriers.

The first three of the above two-phase charge-coupled shift registers can be conveniently implemented by self-aligned, closely spaced structures in the form of polysilicon gates overlapped by aluminum gates (refs. 2-4). In this section we will describe specifically the construction of two-phase CCD's with two different thicknesses of channel oxide for polysilicon and aluminum gates that were used as the test devices in the experimental part of this study. However, in view of these self-aligning characteristics of this structure and the available two-layer metallization, basically the same construction can be used to implement two-phase CCD's employing a dc offset voltage between the adjacent polysilicon and aluminum gates powered by the same phase-voltage pulse train. The externally introduced dc offset voltage, however, can also be replaced by a difference in fixed charge in the channel oxide between the polysilicon and the aluminum gate.

The basic fabrication procedure for the polysilicon-aluminum two-phase CCD is illustrated in Fig. 7. The process is essentially the same as standard silicon-gate processing currently in use by many MOS IC manufacturers. After source/drain diffusions and the definition of some type of channel-confinement structure [Fig. 7(a)], a channel oxide is grown and polysilicon is deposited and defined [Fig. 7(b)]. Then, as shown in Fig. 7(c), a thermal oxide is grown over the polysilicon. This provides the insulation for the polysilicon gates and simultaneously grows a thicker gate oxide in the gaps between the polysilicon gates. Finally, as shown in Fig. 7(d), contact openings are made to the diffusions and polysilicon, and aluminum gates are defined.

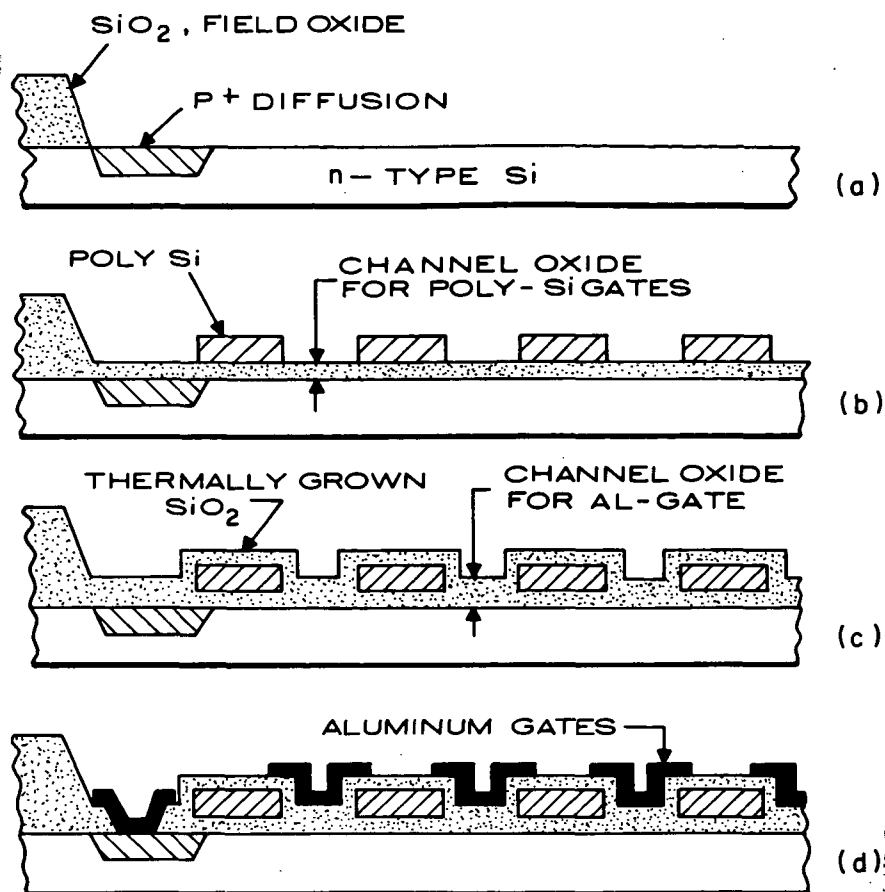


Figure 7. Construction of two-phase charge-coupled devices in the form of polysilicon gates overlapped by aluminum gates.

Note that the gap between adjacent polysilicon and aluminum gates is determined by the thickness of the oxide covering the polysilicon gates [i.e.,  $\sim 2000 \text{ \AA}$  ( $\sim 0.2 \text{ \mu m}$ )]. In three-phase single-level metal CCD structures, this gap spacing is determined by the metal-etching step and is generally on the order of  $2 \text{ \mu m}$  or greater.

Another advantage of this structure is the self-aligning feature of the aluminum gates over the polysilicon gates. Alignment is required only to ensure that the aluminum overlaps the polysilicon on both sides. This also provides a structure that has no exposed channel oxide and is therefore free of any stability problems resulting from the accumulation of ionic charge on such exposed oxides to which single-level metal structures are susceptible.

2. Process Variations. - We have constructed and studied the operation of a variety of p-channel as well as n-channel two-phase CCD's made on substrates with low and high resistivities. Initial test devices were made using n-type substrates with 1.0 ohm·cm resistivity and (111) orientation. Subsequently, most of our p-channel and n-channel CCD's were made on substrates with (100) orientation. This included the devices made using n-type substrates with resistivities of 1.0 and 10 ohm·cm, as well as p-type substrates with resistivities of 1.0 and 30 ohm·cm.

For devices made on 1.0 ohm·cm n-type substrates the channel confinement (defining the width of the channel) was obtained by means of thick-field oxide [ $12\,000\text{-}\text{\AA}$   $\text{SiO}_2$  ( $1.2\text{ }\mu\text{m}$ )] for the substrates with (111) and (100) orientations and by means of a polysilicon field shield for the case of the substrate with (100) orientation. A diffusion guard ring, however, was used to obtain the channel confinement for the p-channel devices made on the 10 ohm·cm substrates.

The n-channel CCD's were made using thick-field oxide for channel confinement in the case of 1.0-ohm·cm substrates and polysilicon field-shield for the case of 1.0- and 30-ohm·cm substrates.

We have used boron deposition, following the standard thick-oxide PMOS process, for the fabrication of  $p^+$ -diffusions for the p-channel CCD's. For more details see ref. 6. The  $n^+$ -diffusions for the n-channel devices as well as the  $n^+$ -diffusion guard rings for the high-resistivity p-channel CCD's were prepared using phosphor-oxychloride as the diffusion sources.

## B. Description of Experimental Devices

1. 64- and 128-Stage Shift Registers. - A photomicrograph of one of the CCD chips used for our experiments is shown in Fig. 8. The data reported here concern the operation of the two middle registers on the chip. They are 64- and 128-stage registers with 1.2-mil-long ( $30\text{-}\mu\text{m}$ -long) stages. The construction of these registers is illustrated in detail in Fig. 9. As is shown, the input structure consists of a source diffusion S-1 and input gates G-1 and G-2. Separate electrical access has also been provided to the polysilicon and aluminum electrodes of each phase, i.e.,  $\phi$ -1 (poly),  $\phi$ -1 (Al),  $\phi$ -2 (poly), and  $\phi$ -2 (Al). The output can be detected as the current flow out of the drain diffusion D-1 or as a voltage change resulting from the charge signal introduced on the floating diffusion that, in turn, controls the gate voltage of a 3-mil-wide ( $75\text{-}\mu\text{m}$ -wide) output MOS device with a source S-2 and drain D-2. The electrodes G-3 and G-4 are externally available for controlling the signal flow in and out of the floating diffusion.



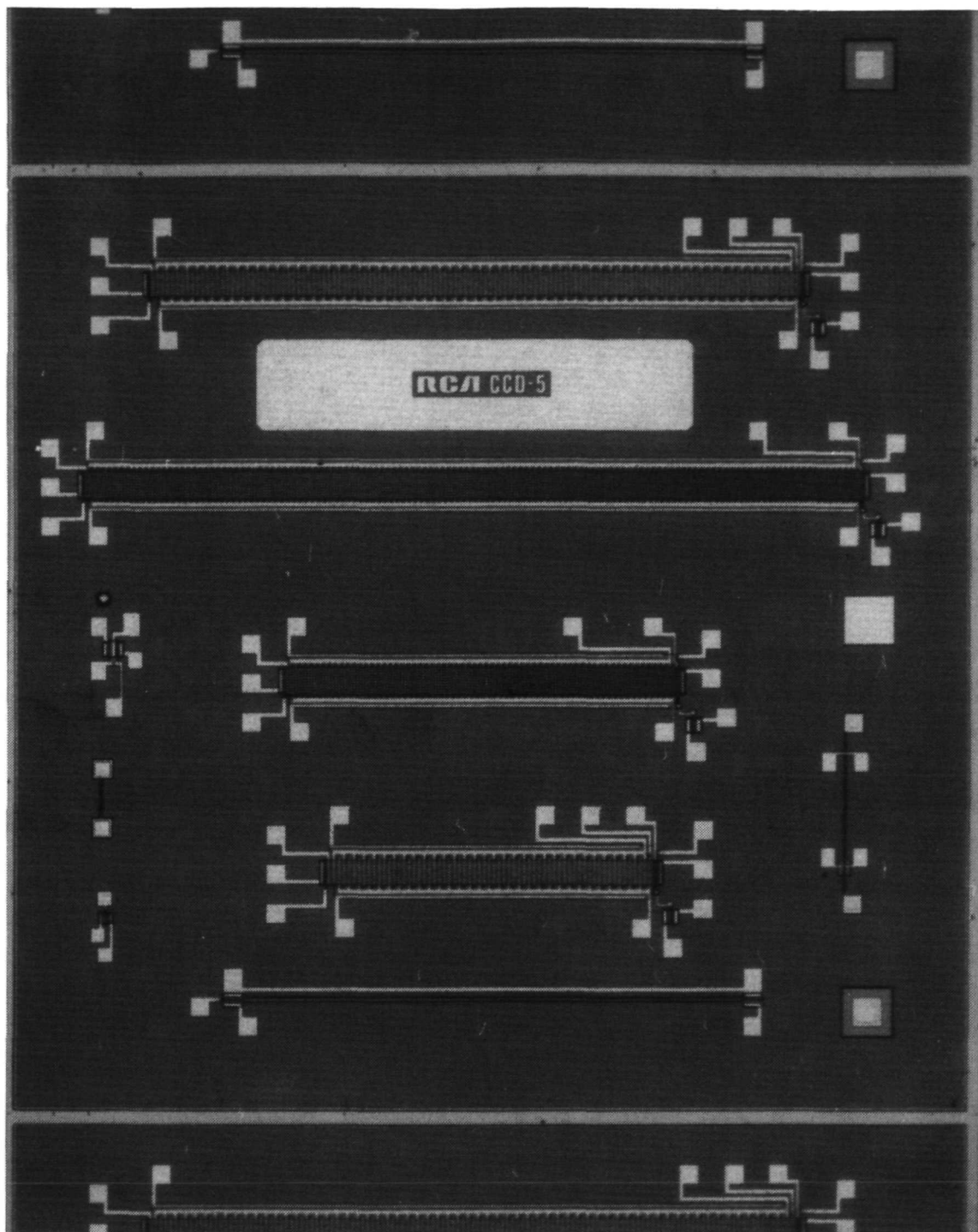


Figure 8. Photomicrograph of CCD-5 chip.

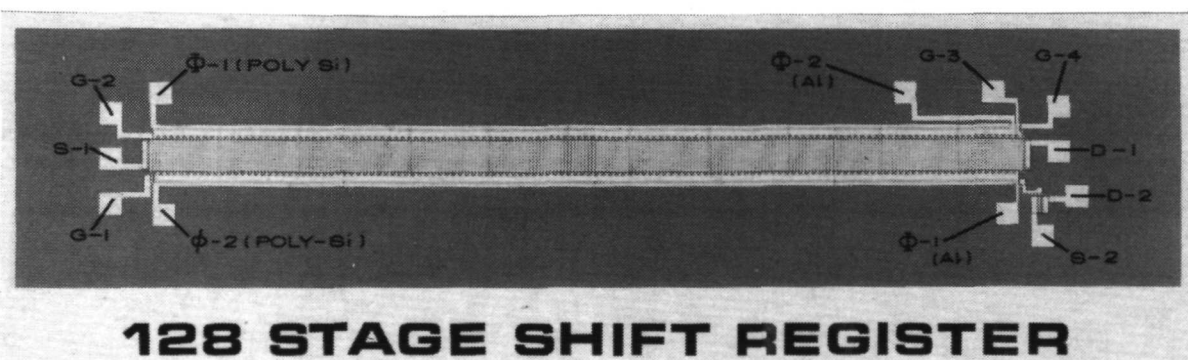
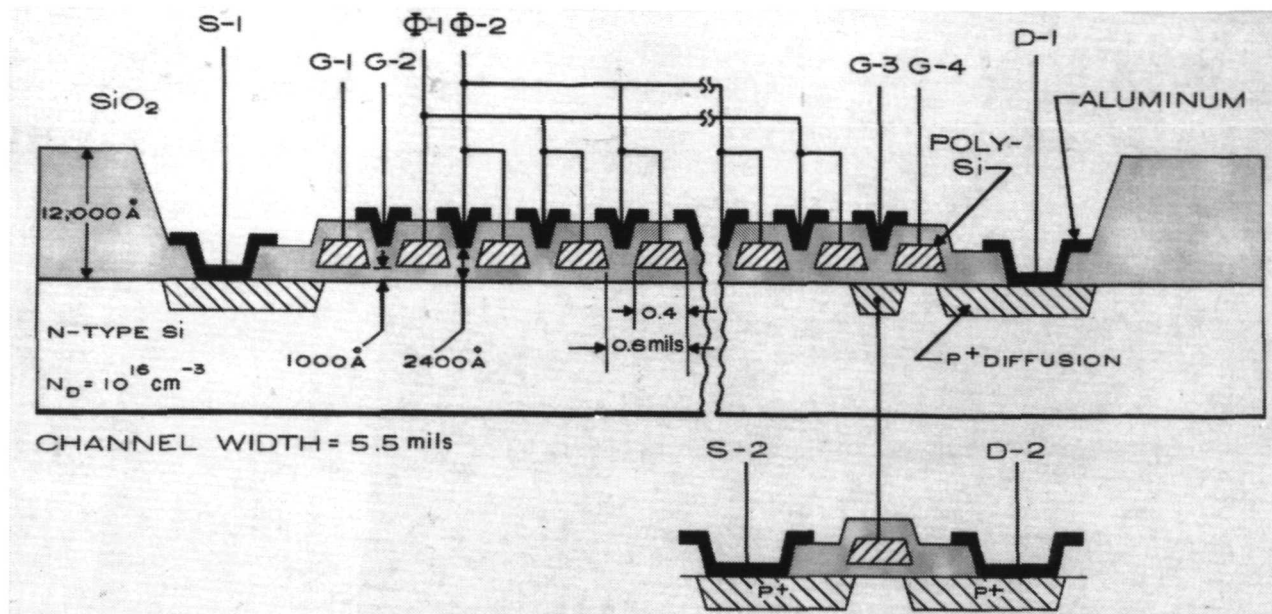


Figure 9. Cross-sectional view and a labeled photograph of the CCD-5 128-stage shift register, 1.2 mils/stage.

The center-to-center spacing of 1.2 mils (30- $\mu\text{m}$ )/stage represents the minimum that can be achieved with 0.2-mil (5- $\mu\text{m}$ ) spaces between lines and 0.1-mil (2.5- $\mu\text{m}$ ) overlap between the polysilicon and aluminum gates.

Unless otherwise designated, most of the devices studied were 5.0 mils (125- $\mu\text{m}$ ) wide. However, to study the effect of the width of the CCD channel on the performance of the registers, special CCD arrays were made, having basically the same layout as is shown in Figs. 8 and 9, but with 0.5- and 1.0-mil-wide (12.5- and 25- $\mu\text{m}$ -wide) channels. In this

case, the 128-stage registers were made 0.5-mil (12.5- $\mu\text{m}$ ) wide and the 64-stage registers were 1.0-mil (25- $\mu\text{m}$ ) wide. Finally, the tested devices were bonded on 28-lead dual-in-line ceramic packages. The bonding arrangement for the 128-stage devices is shown in Fig. 10. The bonding arrangement is identical for the 64-stage devices.

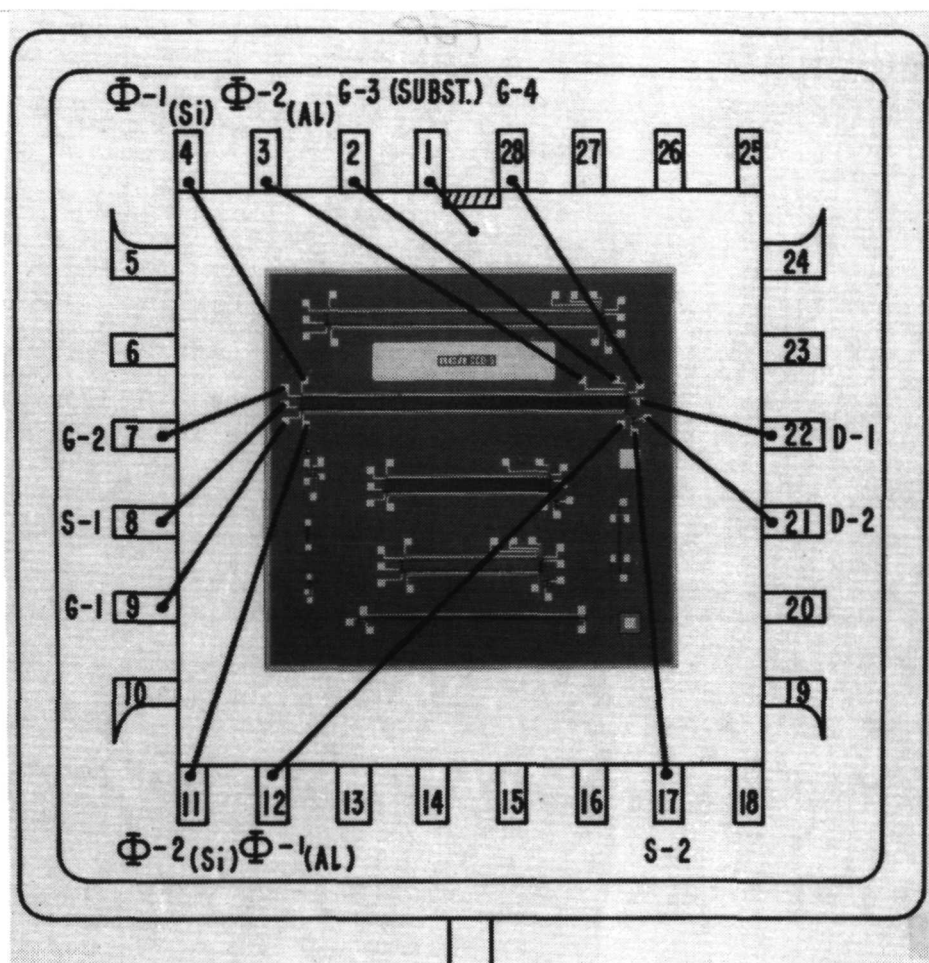
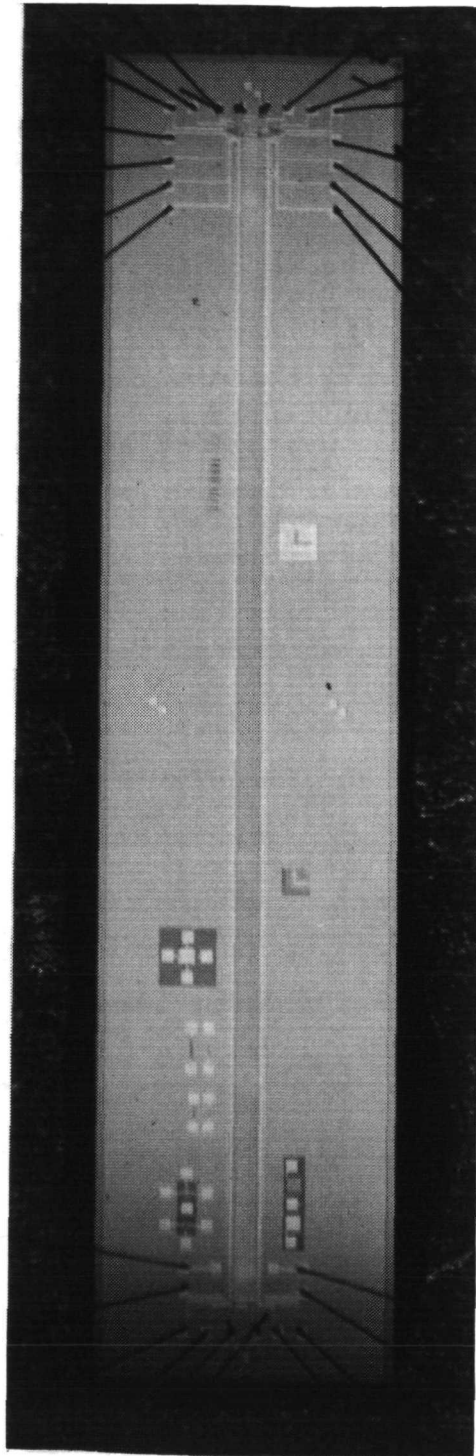


Figure 10. Bonding diagram for the CCD-5 128-stage shift register with 1.2-mil (30- $\mu\text{m}$ ) stages.

At the bottom of the photomicrograph in Fig. 8 is a test device consisting of two MOS devices driven by a common polysilicon gate. This test device was used to verify the expected delay time since the long polysilicon gate behaves as an RC transmission line (see ref. 15).

2. 500-Stage Shift Registers. - While the 500-stage device is essentially just a longer version of the 128-stage device, the sheer length of the 500-stage device required some significant dimensional changes. In particular, the use of the 1.2 mil (30  $\mu\text{m}$ ) per stage dimensions for a 500-stage device results in an overall length in excess of 600 mils (1.5 cm) that exceeds standard mask-making capabilities. Therefore, the 500-stage device was constructed with a 0.8 mil (20- $\mu\text{m}$ ) per stage dimension incorporating a 0.3-mil (7.5- $\mu\text{m}$ ) (in the direction of charge transfer) polysilicon gate with a 0.1-mil (2.5- $\mu\text{m}$ ) gap. The alignment tolerance between aluminum and polysilicon remained at 0.1 mil (2.5  $\mu\text{m}$ ). This reduces the overall device length to about 400 mils (1 cm), resulting in a chip size of 100 mils x 455 mils (0.254 cm x 1.16 cm). Figure 11 is a photomicrograph of the chip. The design incorporates two parallel channels, one 1.0-mil (25- $\mu\text{m}$ ) wide, the other 5.0-mils (125- $\mu\text{m}$ ) wide, driven by the same phase electrodes but with separate inputs and outputs.

Figure 12 shows a schematic cross section through one of the channels. The electrode arrangement and labeling is similar to that of the 128-stage device except that the final number in the label is used to designate either the 1-mil (25- $\mu\text{m}$ ) or the 5-mil (125- $\mu\text{m}$ ) channel. The electrical input stage consists of a source diffusion S-1 and two control gates G-1 and G-2. As with the 128-stage device, the output can be detected as the current flow out of the drain diffusion D-1. On the 500-stage device, the floating diffusion voltage is the input to an inverter in which both transistors have a 0.4-mil (10- $\mu\text{m}$ ) channel length and 3-mil (75- $\mu\text{m}$ ) width. With both transistors operated in saturation, a linear unity-gain transfer function results. The bonding diagram for the 500-stage device is shown in Fig. 13.



1.0mm

Figure 11. Photomicrograph of 500-stage CCD chip.

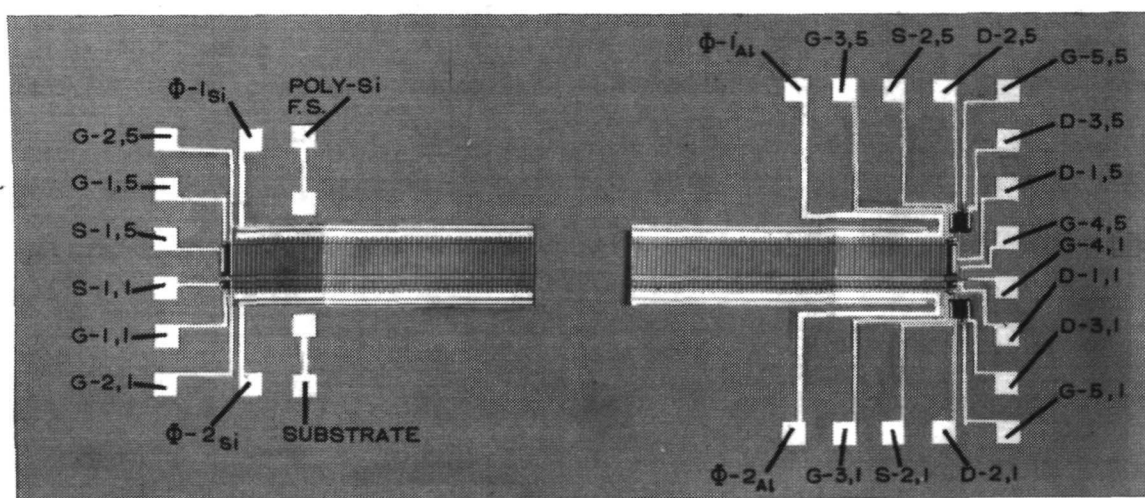
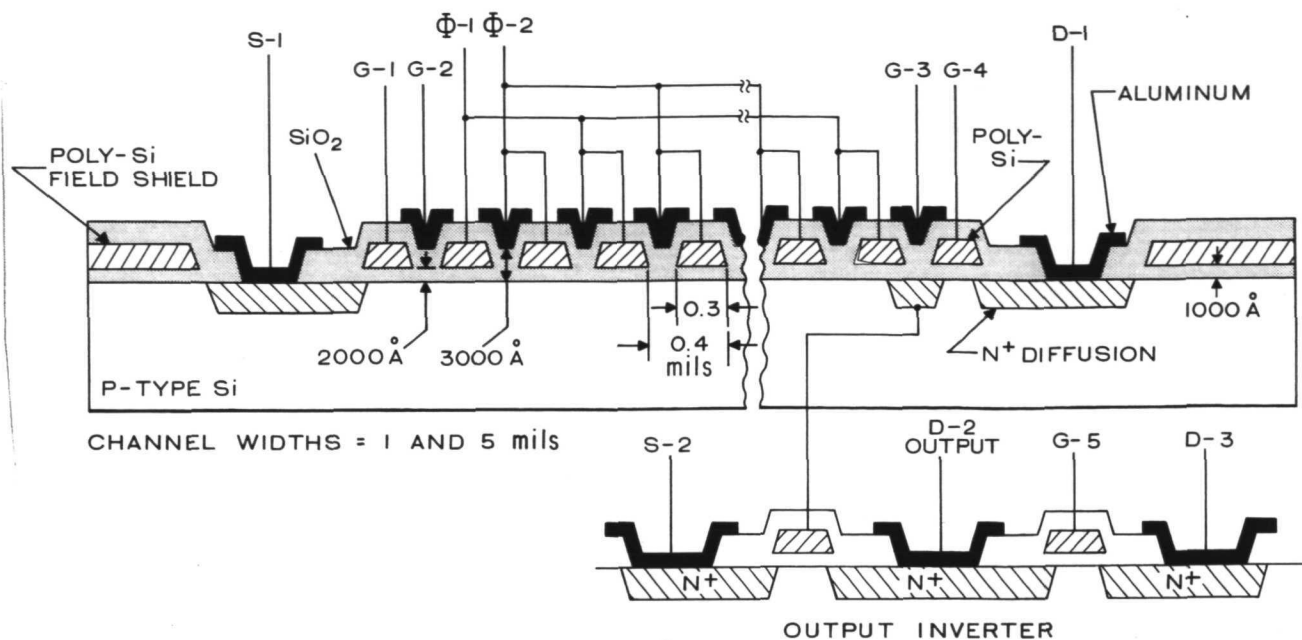


Figure 12. Cross-sectional view and a labeled photograph of the 500-stage shift register.



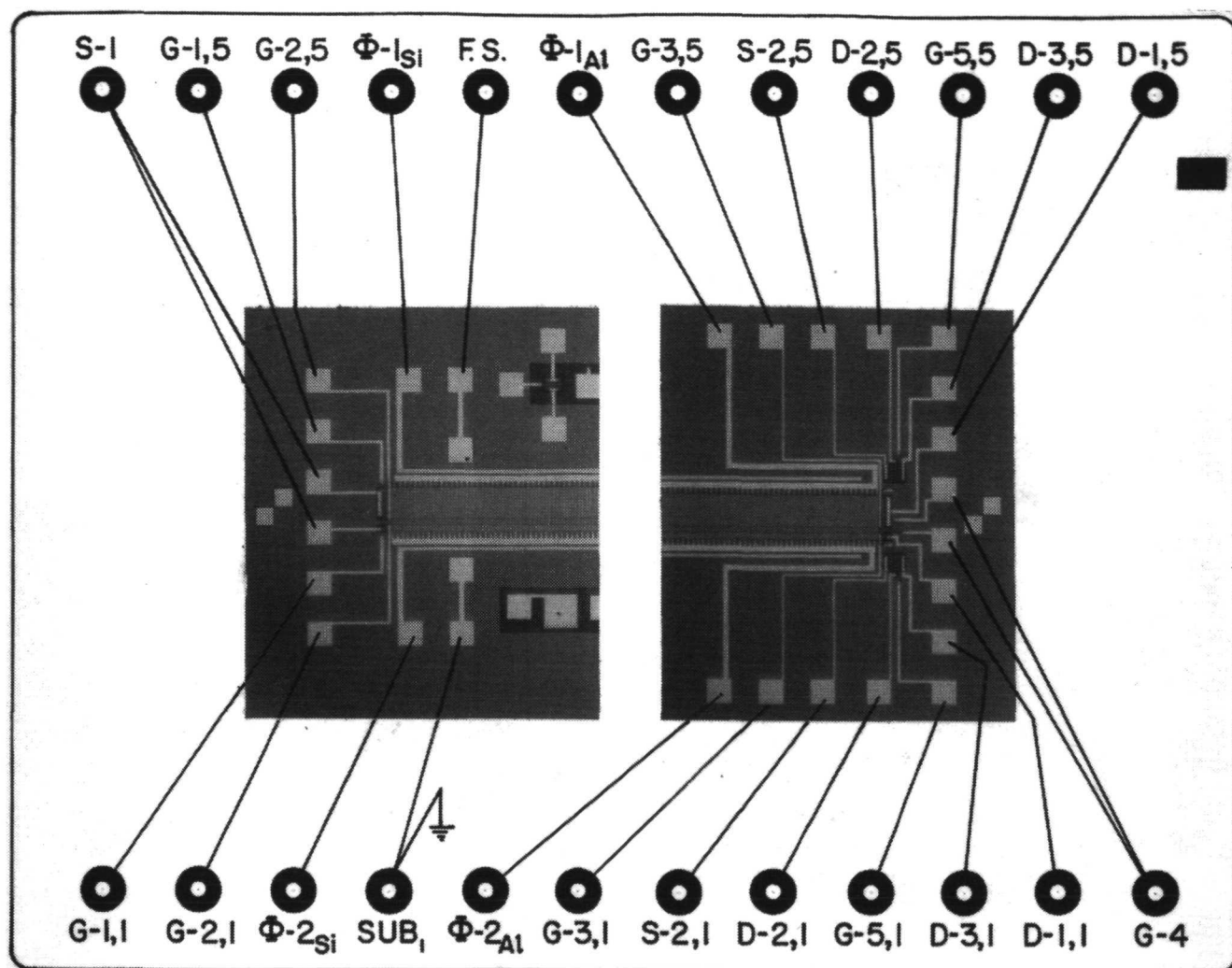


Figure 13. Bonding diagram for the 500-stage shift register.

## IV. EXPERIMENTAL RESULTS

### A. Test Setup

The circuit used for testing the experimental two-phase shift registers is shown in Fig. 14. The input signal is introduced into the

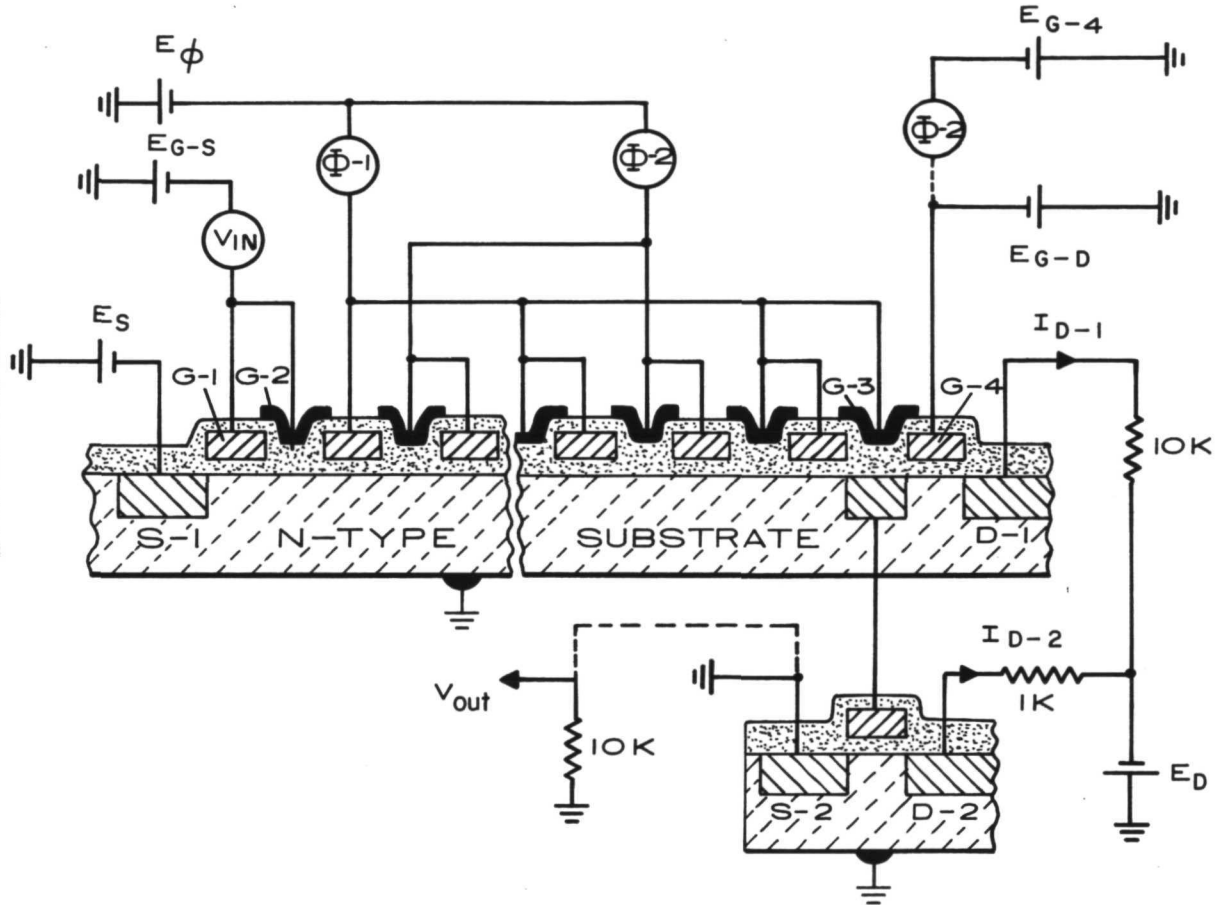


Figure 14. Circuit diagram for the tests of 128-stage two-phase charge-coupled shift registers.

shift register under the control of dc bias voltages  $E_s$  and  $E_{G-S}$  and an input phase  $V_{in}$ . The phase voltage clocks  $\phi-1$  and  $\phi-2$  are applied with dc bias  $E_\phi$ . Not shown in Fig. 14 is the fact that the phase voltages, as well as all of the input and the output control signals, were supplied by separate clamping circuits. This permitted us to use



different dc levels for the polysilicon gates and the aluminum gates. However, for the tests in which polysilicon and aluminum gates were operated with the same dc levels, the phase clocks could be applied directly without the use of clamping circuits; in this case, the  $E_\phi$  was applied as a positive substrate-bias voltage. In all of the tests the output gate G-3 was connected to the phase voltage  $\phi-1$ . The output gate G-4, in the early tests, was dc-biased by the  $E_{G-D}$  voltage with a typical value of -15 V, while the drain voltage was typically  $E_D = -25$  V. In the tests for which most of the data are reported, the output gate G-4 was driven by the  $\phi-2$  clock with  $E_{G-4}$  as the dc bias. In typical operation the output circuit was biased with  $E_{G-4} = 17$  V and  $E_D = 20$  V. Such resetting of the floating diffusion to the drain potential  $E_D$  by periodic pulsing of the gate G-4 was found to improve the operation of the narrow-channel devices, i.e., the registers with 0.5- and 1.0-mil-wide (12.5- and 25- $\mu$ m-wide) channels. This was due to the higher loading of the fixed external capacitance on the floating diffusion, which required more positive resetting.

In some of the tests the output signal was sensed directly as current  $I_{D-1}$ . But we found it more convenient to measure the output signal by observing the potential of the floating diffusion under the G-3 gate, which is proportional to the charge signal. This charge, or voltage sensing, was made by measuring the output either as current  $I_{D-2}$  or as source-follower voltage  $V_{out}$ . A measured transfer curve of the source-follower circuit for typical 5-mil-wide (125- $\mu$ m-wide) 128-stage devices is shown in Fig. 15. This transfer curve was obtained by biasing the gate G-4 with a -10 V relative to the drain D-1 and measuring the source-follower output voltage,  $V_{out}$ , as a function of a dc voltage applied to the drain D-1. Drain D-2 of the source-follower circuit in this test was maintained at -25 V.

## B. Experimental Data

1. Dielectric Strength of Insulating Oxide. - The measurement of the breakdown voltage between the polysilicon and aluminum gates showed that the dielectric strength of the oxide grown on the polysilicon was about the same as that of the oxide grown on the silicon substrate. The breakdown voltage between the aluminum gates and the polysilicon gates insulated by 2000- $\text{\AA}$ -thick (0.2- $\mu$ m-thick) oxide was typically 70 V for negative potentials applied to the aluminum gates and 50 V for positive potentials applied to the aluminum gates. The breakdown for the case when the positive potential was applied to the aluminum gates was preceded by a leakage current on the order of 10 to 20  $\mu$ A. In this case breakdown voltages of 60, 50, and 40 V were observed for insulating-oxide thicknesses of 2500, 2000, and 1200  $\text{\AA}$  (0.25, 0.20, and 0.12  $\mu$ m), respectively.

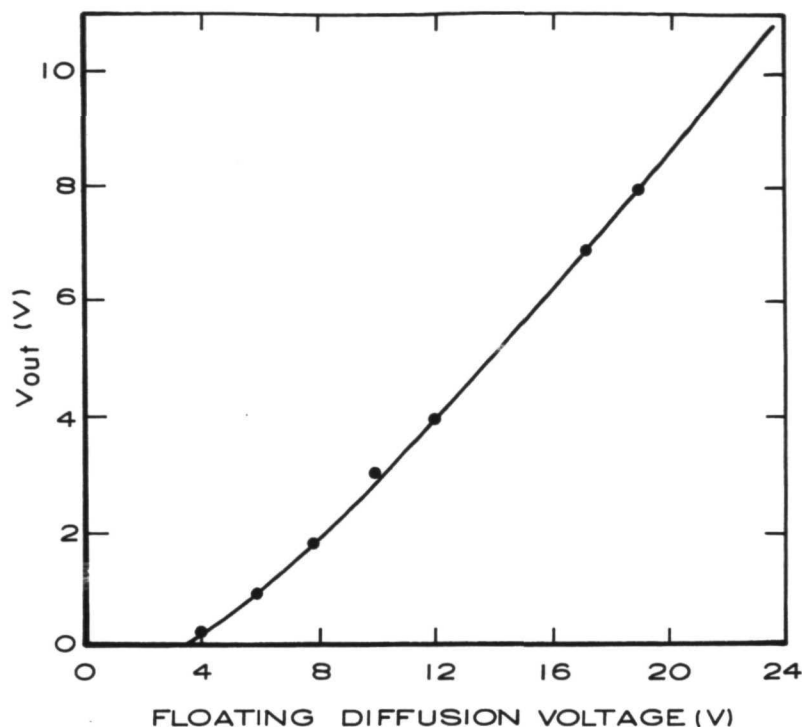


Figure 15. Measured voltage-transfer curve of the source-follower output,  $V_{out}$ , as a function of the voltage on the floating diffusion.

2. Threshold Voltages. - The threshold voltages of the gates could be measured by operating the register as a large, single MOS device. However, the measurement of the threshold voltage that will be reported here consisted of the following procedure: To measure the threshold voltage under the polysilicon gates, the gate G-2 was connected to  $\phi-1$  (see Fig. 9). Then the threshold voltage,  $V_{th}(\text{polysilicon})$ , was measured as the dc voltage applied between gate G-1 and source S-1 that resulted in the introduction of a charge signal into the register on the order of 1% of the full well. During this test, the source S-1 was connected to the substrate. The threshold voltage for the aluminum gates was measured by a similar procedure, by forward-biasing the gate G-1 by 10 V with respect to the source S-1.

Typical threshold voltages measured with 1.0-MHz clock frequency for the reported devices were as follows: For the devices made on 1.0 ohm·cm n-type substrates with (100) orientation,  $V_{th}(\text{polysilicon})$  was typically between -0.6 and -0.9 V and  $V_{th}(\text{aluminum})$  between -2.8 and -3.5 V. For the devices made on 1.0 ohm·cm n-type substrates

with (111) orientation,  $V_{th}(\text{polysilicon})$  was between -1.8 and -2.2 V and  $V_{th}(\text{aluminum})$  between -7.5 and -9.0 V.

The typical threshold voltages for the n-channel devices were  $V_{th}(\text{polysilicon}) = 1.0$  V and  $V_{th}(\text{aluminum}) = +3$  V for 1.0-ohm·cm substrates; and  $V_{th}(\text{polysilicon}) = +1.0$  V and  $V_{th}(\text{aluminum}) = -1.0$  V for the 30-ohm·cm substrates.

3. Thermally Generated Background Charge. - The thermally generated background charge (dark current) was studied by operating the shift registers with interrupted pulse clocks. This type of operation is similar to that of the charge-coupled register as a line sensor, but without the optical input. The clock waveforms used in this test are illustrated in Fig. 16 for the case of the p-channel register. As is shown in this figure, the clock signal is interrupted

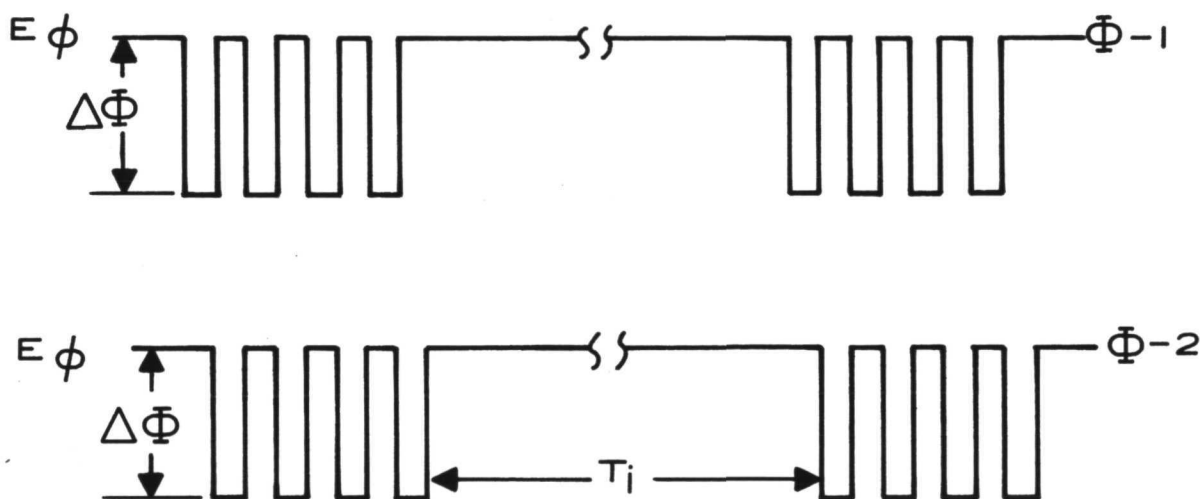


Figure 16. Illustration of clock waveforms for measurements of thermally generated background charge (dark current).

periodically during the charge integration time  $T_i$  while the thermally generated charge is being collected in the potential wells resulting from a constant bias voltage  $E\phi$  applied to both phases of the register. The burst of clock pulses that follows each charge integration time reads out the detected charge signal. Typical waveforms of the detected outputs are shown in Fig. 17 for devices made on (100) substrates.

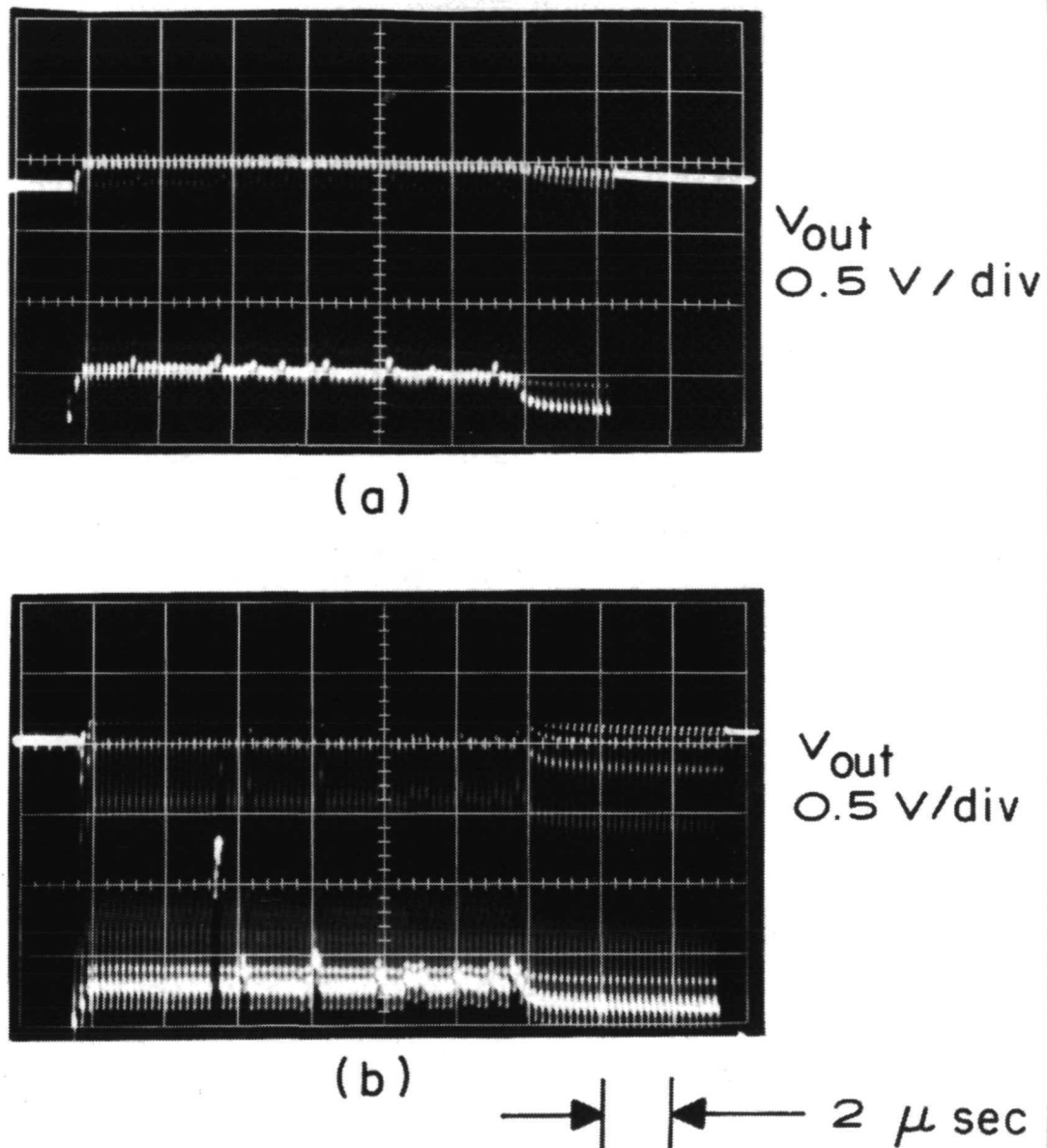


Figure 17. Typical waveforms of thermally generated background charge for 64-stage register operating with phase bias voltage  $E_{\phi} = 5 \text{ V}$ : (a) output for a unit with uniform dark current for  $T_i = 0.25 \text{ sec}$  and (b) output for a unit with large, local dark currents for  $T_i = 10 \text{ msec}$ . The drop in signal corresponds to the end of the register, the edge of the clock feed-through corresponds to the beginning of  $T_i$  as illustrated in Fig. 16.

The waveforms in Fig. 17(a) are for a unit with small uniformly dark current. The waveforms in Fig. 17(b) illustrate the thermally generated charge for a device with local large dark currents.

The variation of the thermally generated background charge as a function of the phase bias (or rather substrate bias) voltage  $E_\phi$  is shown in Fig. 18. Here we see that the uniform-background charge

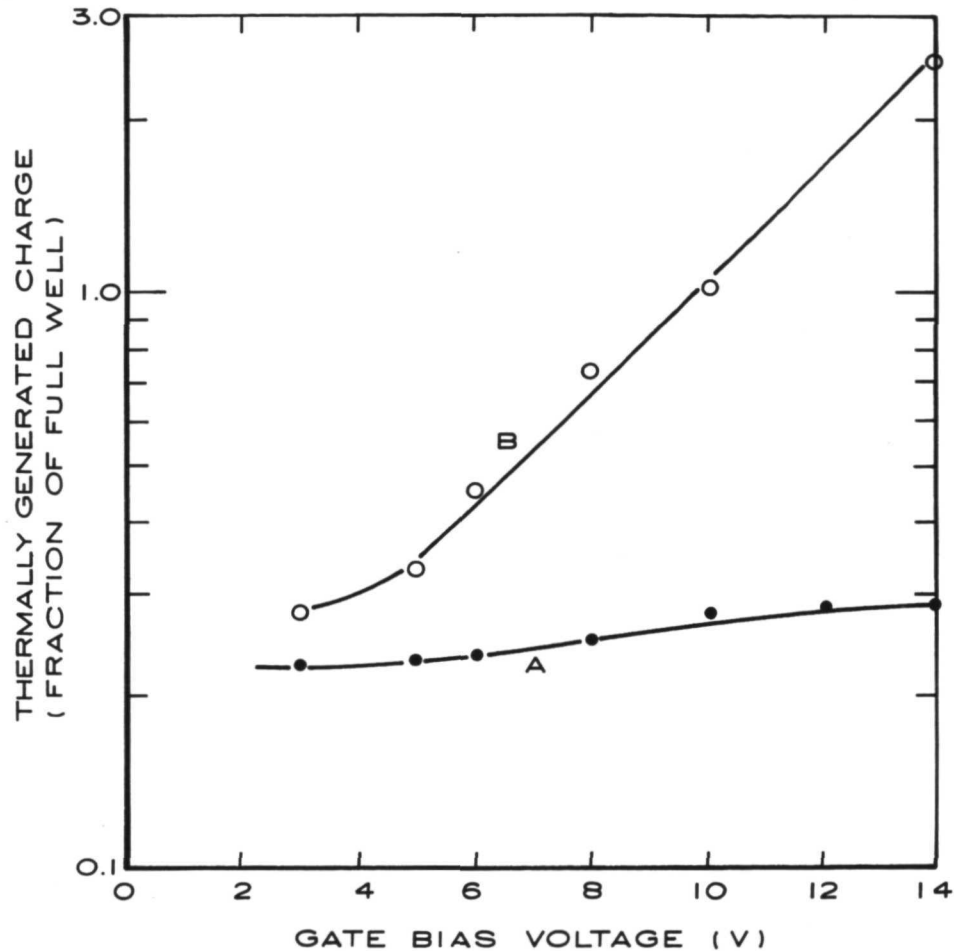


Figure 18. Variation of the thermally generated charge with the gate bias voltage ( $E_\phi$ ) for 64-stage register with large, local dark currents; curve A is for uniform background charge and curve B is for a local dark current spike. Curve A corresponds to the average dark current magnitude as illustrated in Fig. 17(a) while curve B indicates the magnitude of large spikes as seen in Fig. 17(b).

(curve A) changes very slowly with the substrate bias voltage applied during the integration time  $T_i$  [0.25 sec for (a) and 10 msec for (b)]. However, a local high dark-current spike varies exponentially with the bias voltage, as is illustrated by curve B. As the bias voltage changes from 5 to 14 V the locally generated charge changes from about one-third to three full wells. [The data in Figs. 17 and 18 are for a register made on 1.0-ohm·cm n-channel substrate with (100) orientation.]

4. Transfer Loss Measurements. - Unless specifically designated, the transfer measurements reported here are for devices made on 1.0-ohm·cm n-type substrates.

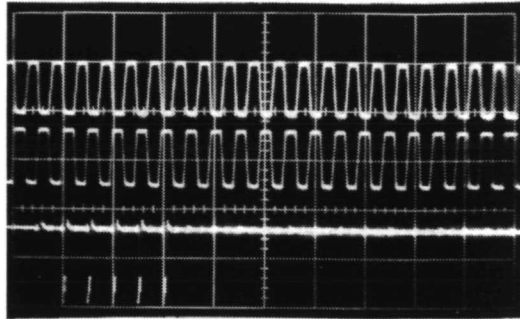
a. Typical Waveforms: Figures 19 through 24 illustrate the waveforms obtained in the measurement of the transfer loss of the two-phase registers. Figures 19 through 22 are for the conventional complete-charge transfer or C-C mode of operation. Typical waveforms obtained for the devices operating in the bucket-brigade or B-B mode are shown in Figs. 23 and 24.\*

The waveforms in Fig. 19 illustrate the operation of a 64-stage register, in which the output gate (see Fig. 14) was biased with a fixed dc voltage  $E_{G-D}$ . The top photograph in Fig. 19 shows the two negative-going clocks along with  $V_{in}$  pulses. The negative  $V_{in}$  pulses occur when  $\phi-1$  is "on" or negative. The two detected outputs  $I_{D-1}$  and  $I_{D-2}$  for the operation, without any electrically introduced background charge, i.e., "no fat zero," are shown in the middle photo. In this case the transfer loss,  $\epsilon$ , due to the charge trapping by the fast interface states is  $\epsilon = 1.4 \times 10^{-2}$ . However, as is shown in the bottom photo, the introduction of the electrically introduced charge, or "fat zero", into the register reduces the transfer loss to  $\epsilon < 10^{-4}$ . The "fat zero" was leaked into the first potential well by adjusting the voltages  $E_s$  and  $E_{G-S}$  (see Fig. 14). The amount of fat zero could be measured on the oscilloscope as seen in Fig. 19. In Fig. 19(b) the no fat zero output falls on the top horizontal grid line. In Fig. 19(c) the fat zero level is seen to be approximately one-third of the way between zero (top horizontal grid line) and full well (second horizontal grid line from the top).

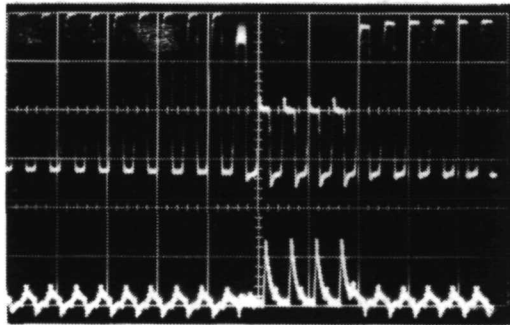
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\*The concept of the C-C and B-B modes of operation of two-phase charge-coupled devices has been described previously in ref. 6 and also discussed in Section V. C.

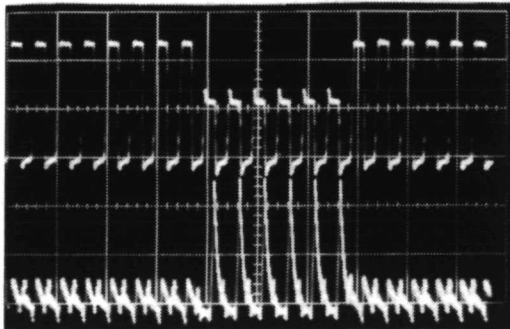
CCD - 6  
64 BIT  
 $f = 1 \text{ MHz}$



$\Phi - 1$   
 $\Phi - 2$  10 V/div  
 $V_{in}$



NO FAT ZERO  
 $\epsilon = 1.4 \times 10^{-2}$   
 $I_{D-2}$  0.5 mA/div  
 $I_{D-1}$  10  $\mu\text{A}/\text{div}$



WITH FAT ZERO  
 $\epsilon < 10^{-4}$   
 $I_{D-2}$  0.5 mA/div  
 $I_{D-1}$  5  $\mu\text{A}/\text{div}$

→ | | ← 2  $\mu\text{sec}$

Figure 19. Typical waveforms for 64-stage register at 1 MHz with (111) substrate orientation.

Measurements of the transfer loss are further illustrated in Fig. 20 for a 64-stage 1.0-mil-wide (25- $\mu$ m-wide) register and in Fig. 21 for a 128-stage 0.5-mil-wide (12.5- $\mu$ m-wide) register. In these two cases, the output signal is detected as the source-follower output,  $V_{out}$ , and the dc voltage of the output gate G-4 was adjusted so that the clock-voltage pickup is cancelled from the output signal.

Inspection of Fig. 20 shows that for "no fat zero" operation, the fractional loss per transfer  $\epsilon = 3.1 \times 10^{-3}$  due to the interface trapping is measured as the loss of the first "1" in the string of "1's". For the measurement of transfer loss for operation with 10% "fat zero",  $\epsilon = 2.3 \times 10^{-4}$  is the loss per transfer measured as the attenuation of the first "1" in the string of "1's" and  $\epsilon = 1.8 \times 10^{-4}$  as the increase of the first "0" following the string of "1's". For this device, according to our definition of the transfer loss, i.e., the loss of the first "1" in a string of "1's", we would choose  $\epsilon = 2.3 \times 10^{-4}$  as the value for transfer loss. However, as the value of fat zero is increased, the same transfer loss would be measured as either the reduction of the first "1" in the string of "1's" or as the increase of the first "0" following the string of "1's". Such measurement is illustrated in Fig. 21(c). Comparison of the waveforms in parts (b) and (c) of Fig. 21 illustrates the reduction in the transfer loss as the signal is reduced for a given value of fat zero, substantiating Eq. (13).

The operation of the same 64-stage register (CCD-6-5-8) in the C-C and B-B modes is illustrated by Figs. 22, 23, and 24. E represents the dc voltages applied to the polysilicon gates in excess of that applied to the A1-gate. The comparison of the waveforms shows that the operation in the B-B mode with larger barrier heights leads to larger transfer losses with and without "fat zero".

b. Transfer Loss as Function of Fat Zero: The reduction of the transfer loss as the function of fat zero is illustrated in Fig. 25. The comparison of curve A for C-C mode with curves B and C for B-B modes shows that about 10% of fat zero reduces the transfer loss to a minimum value in the case of B-B mode, but the minimum loss for the C-C mode requires a larger value of fat zero.

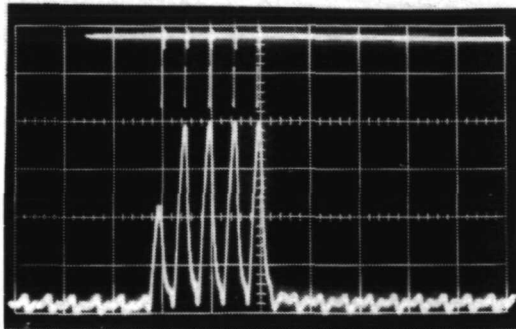
Figure 26 shows how the transfer loss as a function of fat zero varies with the channel width. The curves on this figure illustrate the edge effect that becomes more important in the case of the narrower devices.

c. Transfer Loss as a Function of Clock Frequency: The measurements of the transfer loss as function of clock frequency are shown in



CCD 5-3-10  
64 BIT  
1.0 mil CHANNEL

NO FAT ZERO



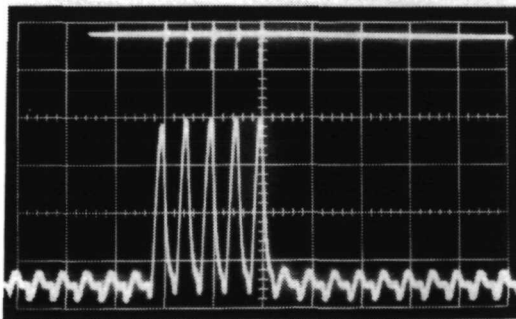
$V_{in}$  2 V/div

$V_{out}$  50 mV/div

$\epsilon = 3.1 \times 10^{-3}$

(a)  $\rightarrow \leftarrow 2 \mu\text{sec}$

10 % FAT ZERO

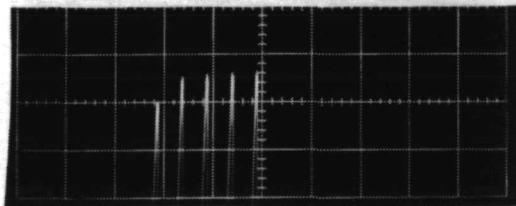


$V_{in}$  2 V/div

$V_{out}$  50 mV/div

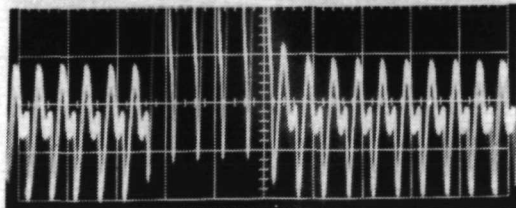
$V_{out}(1)$  10 mV/div

$\epsilon = 2.3 \times 10^{-4}$



$V_{out}(0)$  10 mV/div

$\epsilon = 1.8 \times 10^{-4}$

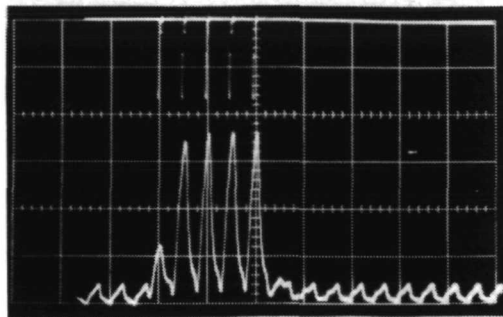


(b)

Figure 20. Waveforms for a 1.0-mil-wide (25- $\mu\text{m}$ -wide) 64-stage register at 1 MHz; (100) substrate.

CCD5-3-21  
128 BIT  
0.5 mil CHANNEL

NO FAT ZERO



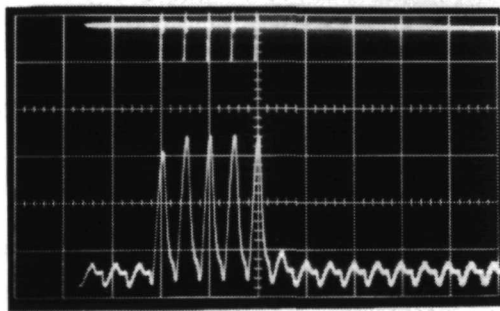
(a)

$V_{in}$  2V/div

$V_{out}$  50 mV/div

$$\epsilon = 2.85 \times 10^{-3}$$

12% FAT ZERO

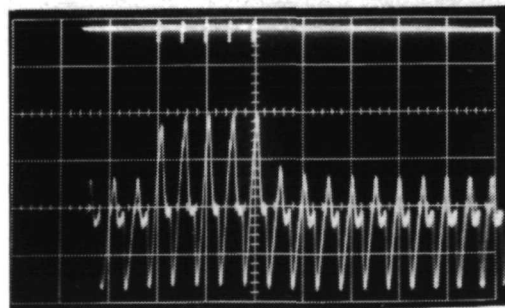


(b)

$V_{out}$  50 mV/div

$$\epsilon = 4.3 \times 10^{-4}$$

12 % FAT ZERO



(c)

$V_{out}$  10 mV/div

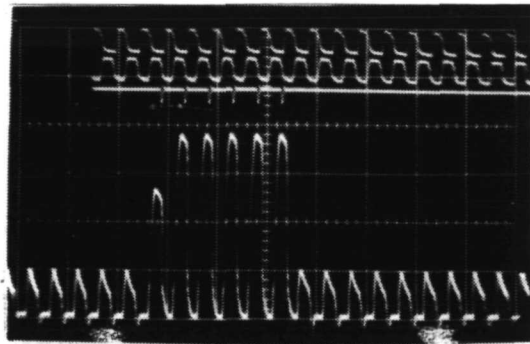
$$\epsilon = 2.8 \times 10^{-4}$$

2  $\mu$  sec

Figure 21. Waveforms for a 0.5-mil-wide (12.5- $\mu$ m-wide) 128-stage register at 1 MHz; (100) substrate.

CCD 6-5-8  
64-BIT  
C-C MODE ( $E=0$ )

NO FAT ZERO

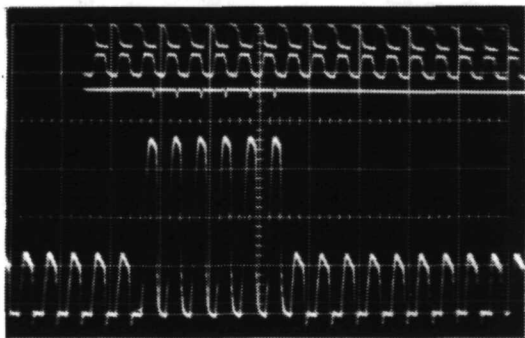


$\phi-1$  20 V/div  
 $\phi-2$   
 $V_{in}$  5 V/div

$V_{out}$  0.5 V/div  
 $\epsilon = 2.86 \times 10^{-3}$

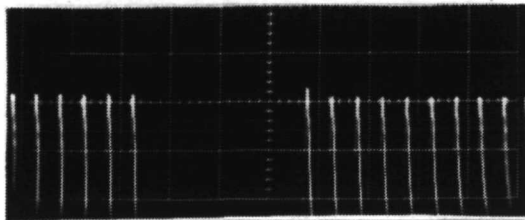
(a)

20 % FAT ZERO



$V_{out}$  0.5 V/div

(b)



$V_{out}$  0.05 V/div

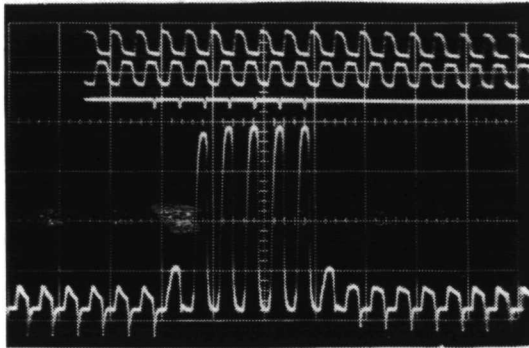
$\epsilon = 5 \times 10^{-5}$

(c)  $\rightarrow \leftarrow 2 \mu\text{sec}$

Figure 22. Waveforms for a 5-mil-wide (125- $\mu\text{m}$ -wide) 64-stage register operating in C-C mode at 1.0 MHz for  $E_{\phi} = 5$  V,  $\Delta\phi = 10$  V,  $E = 0$ ,  $E_{G4} = 17$  V, and  $E_D = 20$  V [substrate (100)].

CCD6-5-8  
64 BIT  
B-B MODE (E=5V)

NO FAT ZERO



(a)

$\phi-1$  20 V/div

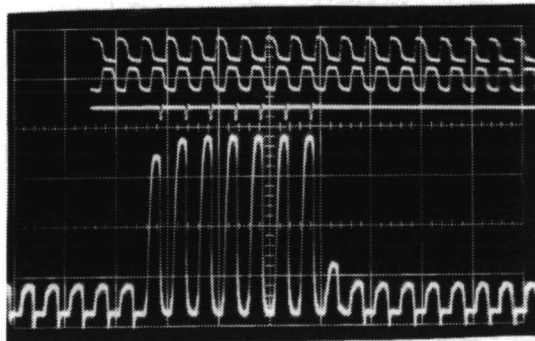
$\phi-2$

$V_{IN}$  10 V/div

$V_{out}$  1.0 V/div

$\epsilon = 1.4 \times 10^{-2}$

10% FAT ZERO



(b)

$V_{in}$  5 V/div

$V_{out}$  1 V/div

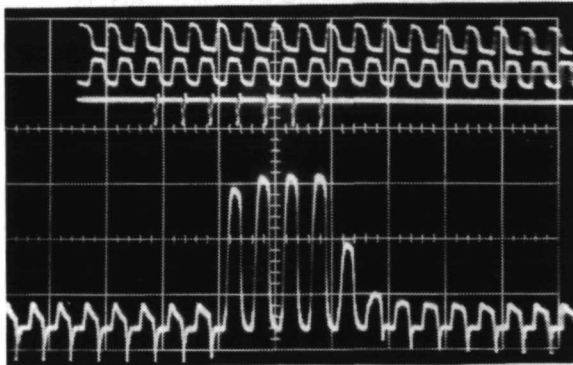
$\epsilon = 1.3 \times 10^{-3}$

→ | ← 2  $\mu$ sec

Figure 23. Waveforms for a 64-stage register of Fig. 22, but operating in B-B mode at 1.0 MHz, with  $E_{\phi} = 5$  V,  $\Delta\phi = 10$  V,  $E = 5$  V,  $E_{G4} = 17$  V, and  $E_D = 20$  V.

CCD 6-5-8  
64 BIT  
B-B MODE ( $E=10V$ )

NO FAT ZERO



(a)

$\phi - 1$  20 V/div

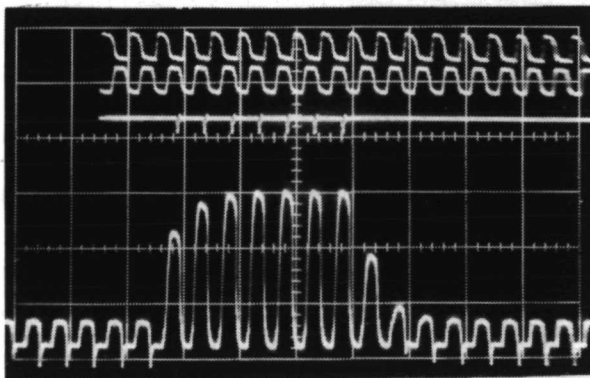
$\phi - 2$

$V_{in}$  1 V/div

$V_{out}$  1 V/div

$$\epsilon = 2.4 \times 10^{-2}$$

10% FAT ZERO



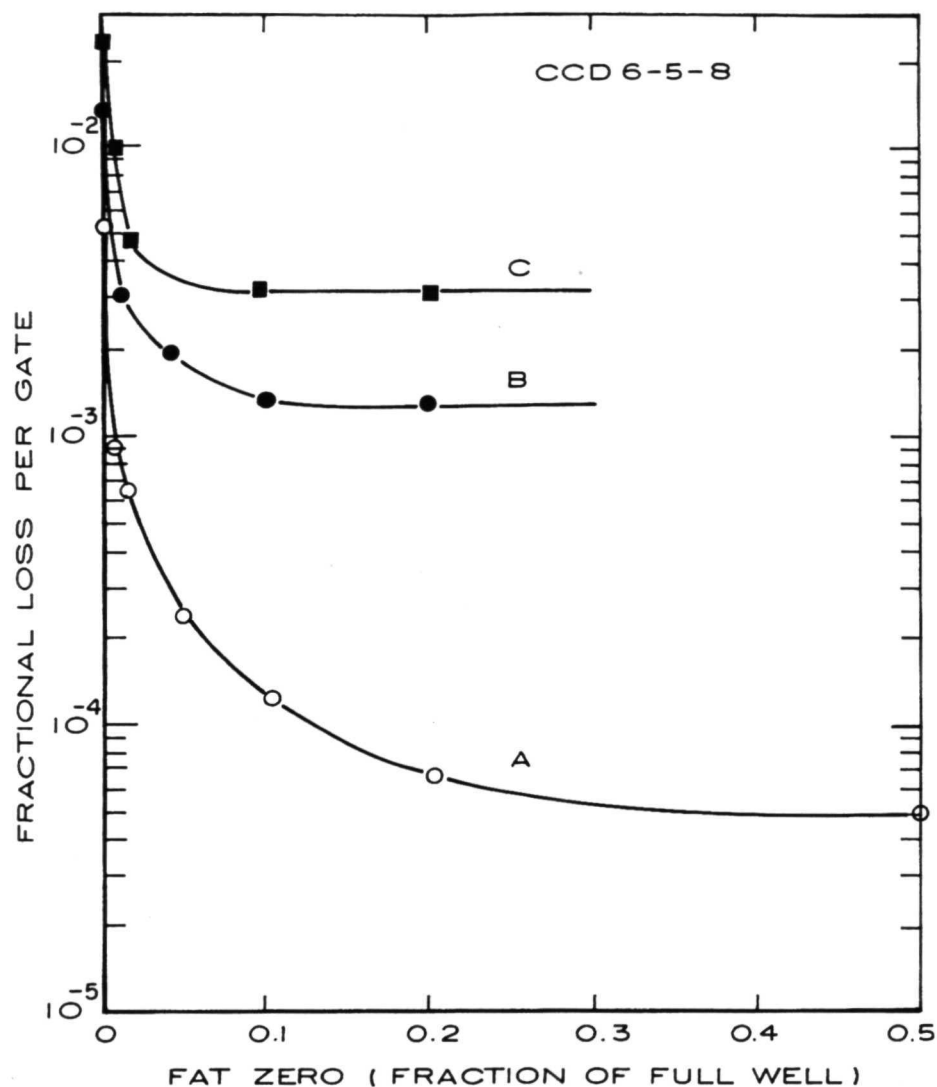
(b)

$V_{out}$  1 V/div

$$\epsilon = 3.2 \times 10^{-3}$$

→ | ← 2  $\mu$ sec

Figure 24. Waveforms for the 64-stage register of Fig. 22, but operating in B-B mode at 1 MHz with  $E_{\phi} = 5V$ ,  $\Delta\phi = 10V$ ,  $E = 10V$ ,  $E_{G4} = 17V$ , and  $E_D = 20V$ .



Curve A: C-C mode,  $E_{\phi} = 5$  V,  $E = 0$  V, and  $\Delta\phi = 10$  V.

Curve B: B-B mode,  $E_{\phi} = 5$  V,  $E = 5$  V, and  $\Delta\phi = 10$  V.

Curve C: B-B mode,  $E_{\phi} = 5$  V,  $E = 10$  V, and  $\Delta\phi = 10$  V.

Figure 25. Fractional loss per transfer versus amount of fat zero for 5-mil-wide (125- $\mu$ m-wide) 64-stage register; (100) substrate.

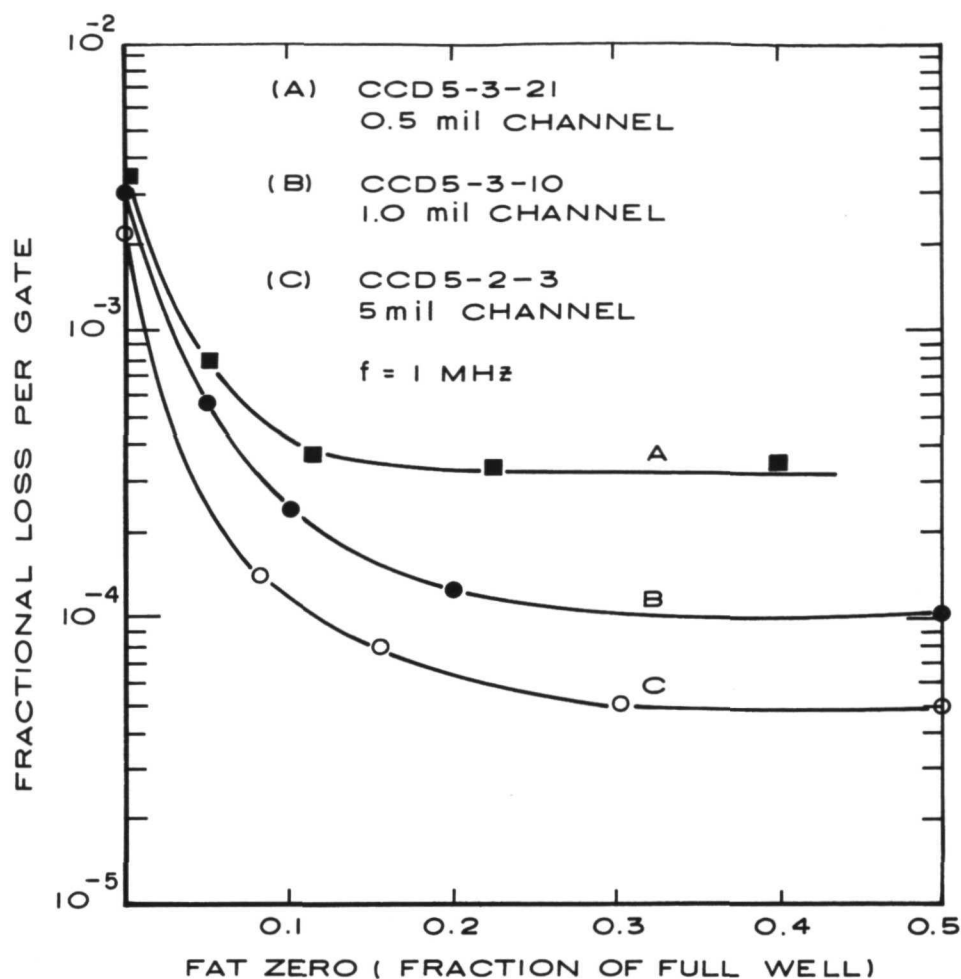
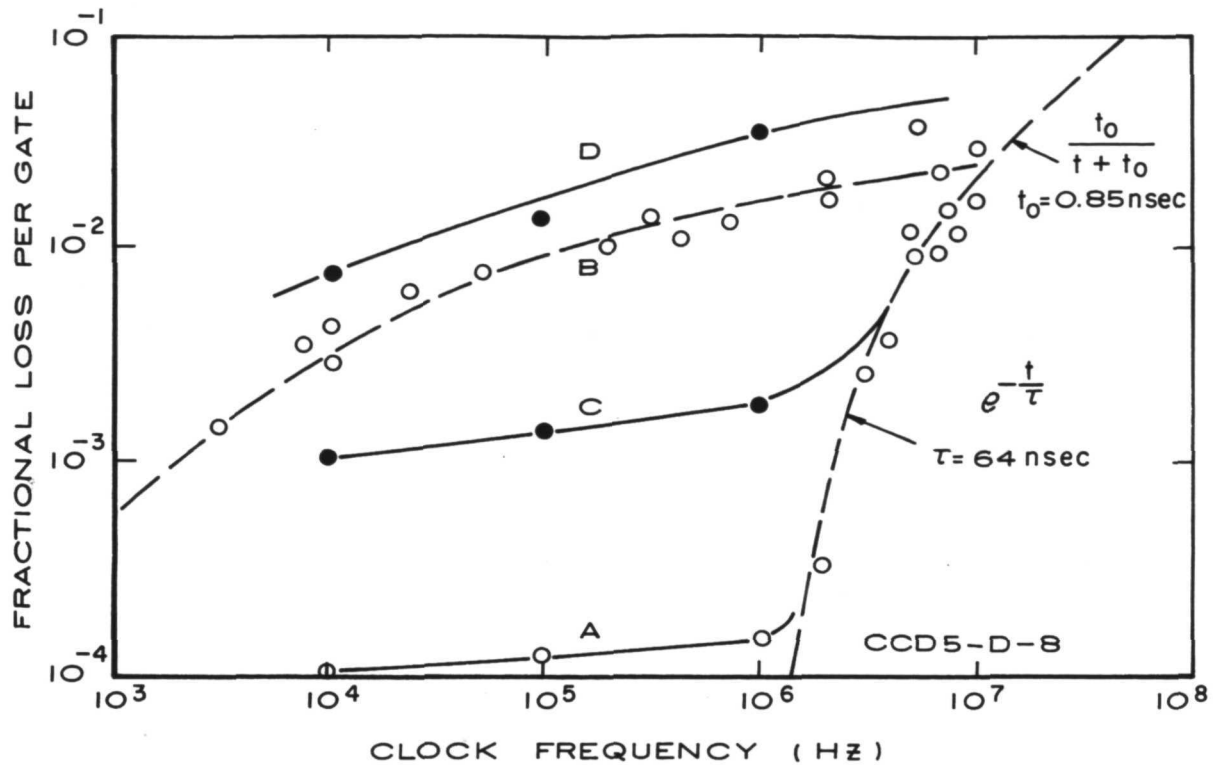


Figure 26. Fractional loss per transfer at 1 MHz versus amount of fat zero for 0.5-, 1.0-, and 5.0-mil-wide (12.5-, 25-, and 125- $\mu\text{m}$ -wide) registers made on (100) substrates are shown as curves A, B, and C, respectively (C-C mode).

Fig. 27 for devices fabricated on (111) substrates. The dotted curve B represents the best fit to the data of the calculated fast interface state trapping losses according to the following equation

$$\epsilon_S = \frac{(kT/q)N_{SS}}{N_{SIG}} \ln\left(1 + \frac{f}{f_0}\right) \quad (18)$$



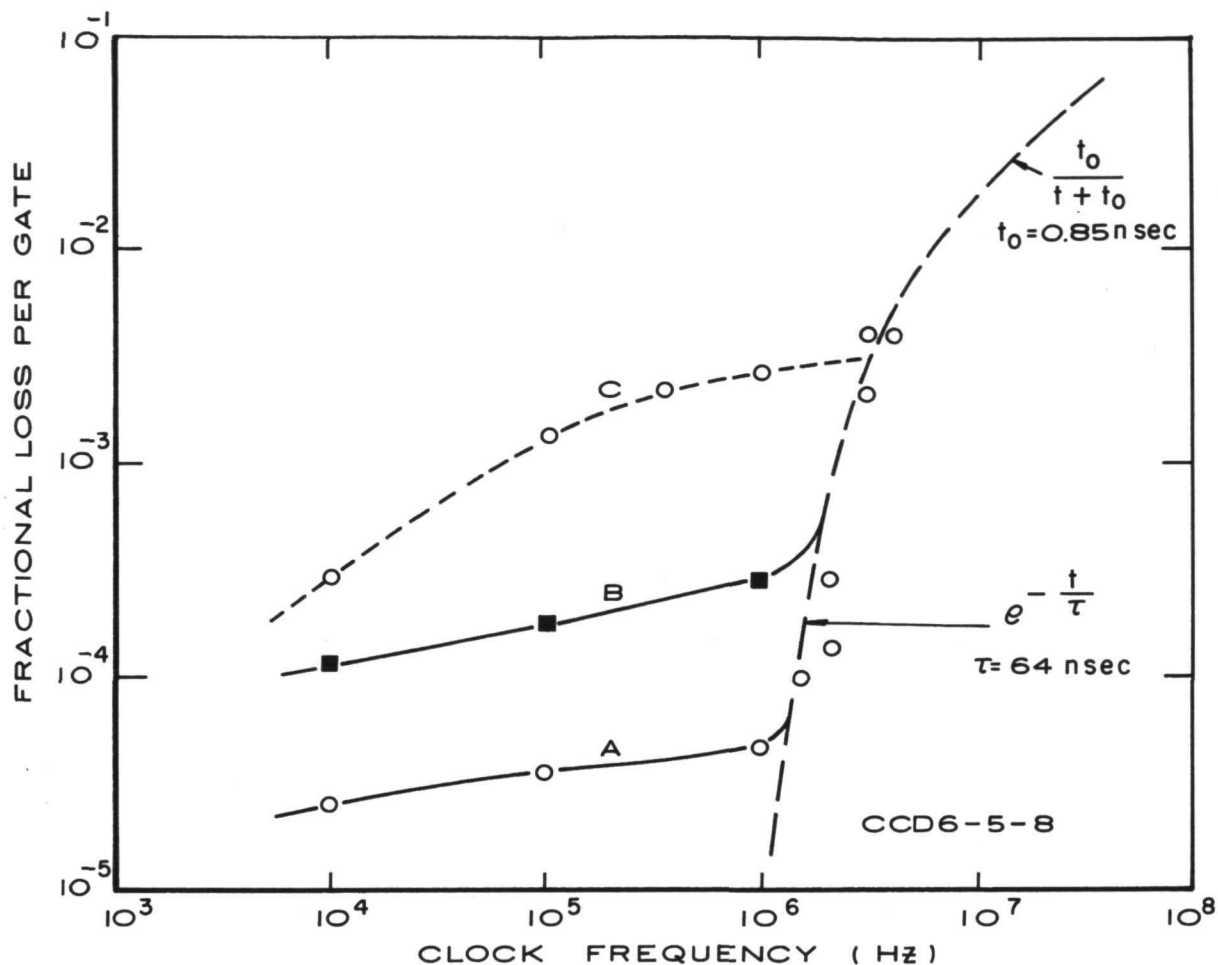
- Curve A: C-C mode ( $E_\phi = 20 \text{ V}$ ,  $E = -5 \text{ V}$ ,  $\Delta\phi = 10 \text{ V}$ ) with 10% fat zero  
 Curve B: C-C mode with no fat zero.  
 Curve C: B-B mode ( $E_\phi = 10 \text{ V}$ ,  $E = 5 \text{ V}$ ,  $\Delta\phi = 10 \text{ V}$ ) with 10% fat zero  
 Curve D: B-B mode with no fat zero.

Figure 27. Fractional loss per transfer versus clock frequency for 128-stage registers made on (111) substrates.

From these data we estimate fast interface state densities of  $N_{ss} = 1.2 \times 10^{11} (\text{cm}^2 \cdot \text{eV})^{-1}$  for the devices made on silicon with (111) orientation. According to these measurements, the transfer loss with fat zero also decreases as a function of clock frequency for both the C-C mode and the B-B modes. The dotted curve on the right represents the calculated transfer loss for free-charge transfer for a 0.4-mil-long ( $10\text{-}\mu\text{m}$ -long) storage gates assuming self-induced drift dominates transfer for the first 99%, with a characteristic time  $t_0 = 0.75 \text{ nsec}$ , and thermal diffusion dominates thereafter with a time constant of 64 nsec appropriate for  $L = 0.4 \text{ mil}$  ( $10 \mu\text{m}$ ) (ref. 7).



The variation of transfer loss curves for the C-C mode for registers made on (100) substrates is shown in Fig. 28. Here again, the



Curve A: 5.0-mil-wide (125- $\mu$ m-wide) 64-stage register with 50% fat zero.

Curve B: 0.5-mil-wide (12.5- $\mu$ m-wide) 128-stage register with 30% fat zero.

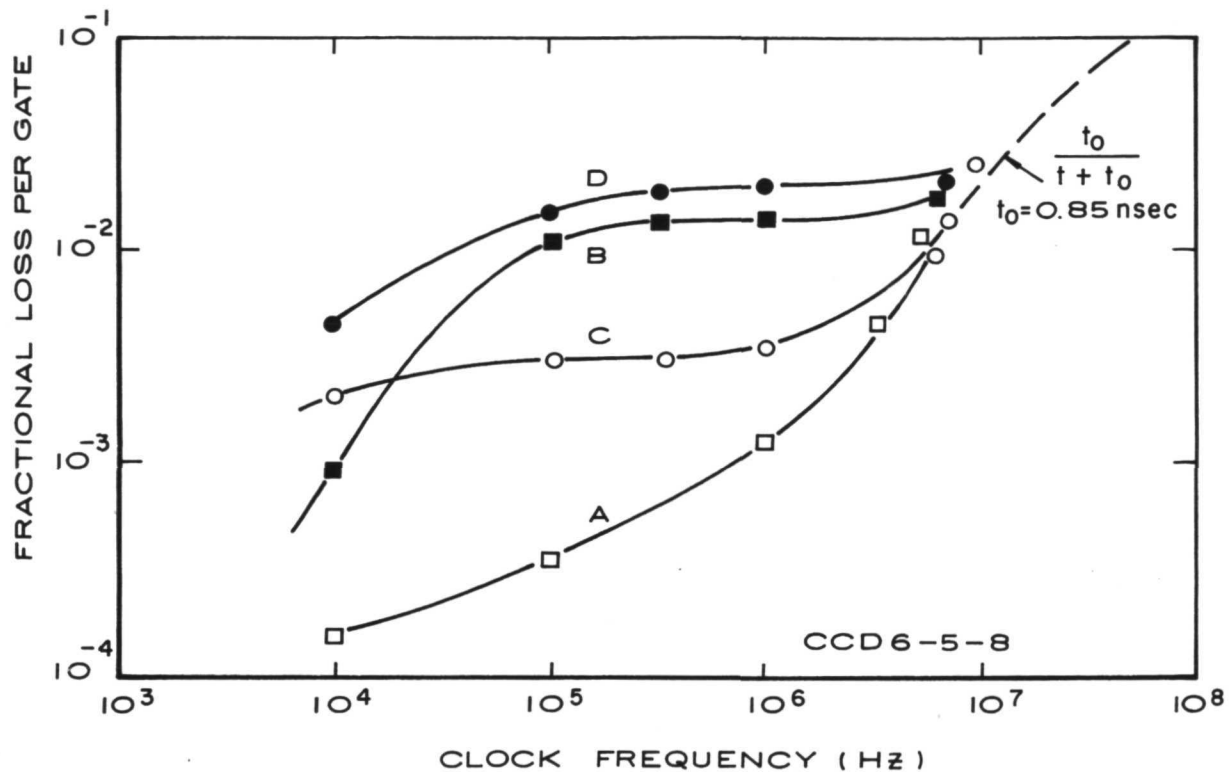
Curve C: 5.0-mil-wide (125- $\mu$ m-wide) 64-stage register with no fat zero.

Figure 28. Fractional loss versus clock frequency for registers made on (100) substrates operating in C-C mode ( $E_{\phi} = 5$  V,  $E = 0$  V,  $\Delta\phi = 10$  V).

best fit to data points for curve C indicates  $N_{SS} = 2.9 \times 10^{10} \text{ (cm}^2 \cdot \text{eV)}^{-1}$ . Curve A shows the transfer loss for a 0.5-mil-wide (12.5- $\mu$ m-wide)

register and 50% fat zero. Curve B shows the transfer loss for a 0.5-mil (12.5- $\mu\text{m}$ ) register with 30% fat zero.

The transfer loss for registers made on (100) substrates operated in the B-B mode with two different barrier heights is shown in Fig. 29. Note that the registers operated in the B-B mode with relatively small barriers have transfer losses that decreased as the clock frequency was reduced.



- Curve A:  $E_\phi = 5 \text{ V}$ ,  $E = 5 \text{ V}$ ,  $\Delta\phi = 10 \text{ V}$ , and 10% fat zero.
- Curve B: Same as A, but with no fat zero.
- Curve C:  $E_\phi = 5 \text{ V}$ ,  $E = 10 \text{ V}$ ,  $\Delta\phi = 10 \text{ V}$ , and 10% fat zero.
- Curve D: Same as C but with no fat zero.

Figure 29. Fractional loss versus clock frequency for 5-mil-wide (125- $\mu\text{m}$ -wide) 64-stage registers made on (100) substrate operating in B-B modes.

d. Transfer Loss as a Function of Substrate Doping: The data on the transfer loss reported in the previous section were obtained on devices made on n-type substrates with 1.0-ohm $\cdot\text{cm}$  resistivities. The

curves of transfer loss versus clock frequency for devices made on low- and high-resistivity n-type as well as p-type substrates are shown in Fig. 30. The data shown in this figure were obtained for no fat zero

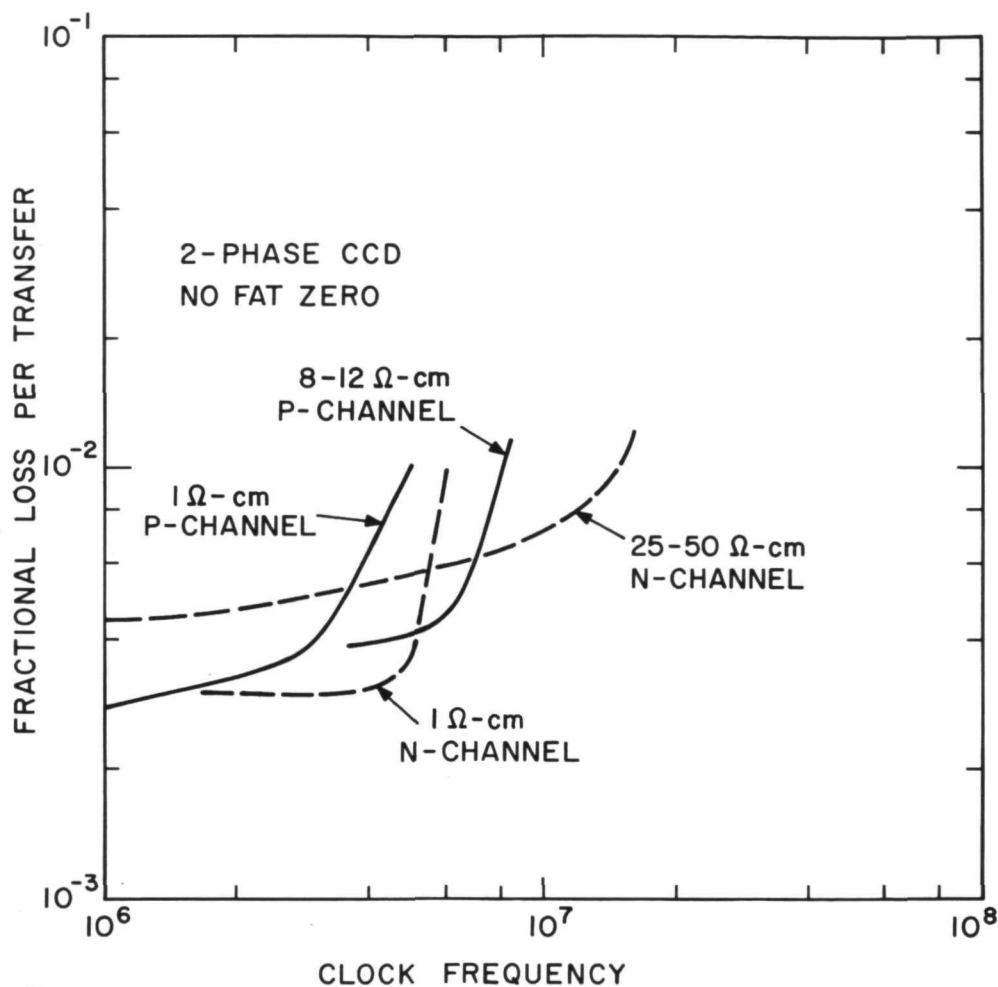


Figure 30. Transfer loss vs. frequency for devices operating without fat zero. The frequency at which the loss per transfer increases abruptly indicates the onset of significant incomplete free-charge transfer.

operation in order to clearly measure the intrinsic speed limitations (due to free-charge transfer) of these devices. The transfer loss data for operation with 20 to 30% fat zero for various two-phase registers operating with 1.0-MHz clock frequency is summarized in Table I.

TABLE I  
Performance of the Tested Two-Phase CCD Registers  
at 1.0-MHz Clock Frequency

No.	Substrate			Channel Confinement	Channel Width [mils ( $\mu\text{m}$ )]	Transfer Loss Per Gate With 20-30% Fat Zero	$N_{ss}$ ( $\text{cm}^2 \cdot \text{eV}^{-1}$ )
	Type	Resistivity ( $\text{ohm} \cdot \text{cm}$ )	Orientation				
1	n	1.0	111	Thick Oxide	5.0(125)	$1.2 \times 10^{-4}$	$8 \times 10^{10}$
2	n	1.0	100	Thick Oxide F.S.	5.0(125)	$5.0 \times 10^{-5}$	$2 \times 10^{10}$
3	n	1.0	100	Thick Oxide F.S.	1.0(25)	$1.0 \times 10^{-4}$	-
4	n	1.0	100	Thick Oxide F.S.	0.5(12.5)	$3.5 \times 10^{-4}$	-
5	n	8-12	100	Diffusion Guard Ring	5.0(125)	$2.0 \times 10^{-4}$	-
6	p	1.0	100	Thick Oxide	5.0(125)	$< 10^{-4}$	-
7	p	1.0	100	Thick Oxide	0.5(12.5)	$2 \times 10^{-4}$	-
8	p	25-50	100	Poly-Si Field Shield	5.0(125)	$3 \times 10^{-4}$	-
9	p	25-50	100	Poly-Si Field Shield	0.5	$1.2 \times 10^{-3}$	-
10	p	1.0	100	Poly-Si Field Shield	5.0(125)	-	-
11	p	1.0	100	Poly-Si Field Shield	1.0(25)	$2 \times 10^{-4}$	-
12	p	30	100	Poly-Si Field Shield	5.0(125)	-	-
13	p	30	100	Poly-Si Field Shield	1.0(25)	-	-

Devices 1 to 9 were 64- and 128-stage registers with 0.4-mil (10- $\mu\text{m}$ ) polysilicon gates and 0.2-mil (5- $\mu\text{m}$ ) aluminum gates.

Devices 10 to 13 were 500-stage registers with 0.3-mil (7.5- $\mu\text{m}$ ) polysilicon gates and 0.1-mil (2.5- $\mu\text{m}$ ) aluminum gates.

This low-frequency performance for fat zero operation can be explained by edge effects (see Section IV. B.) and other losses connected with charge trapping by the fast interface states (see Section II. B).

### C. Experimental Results of 500-Stage Register

1. Transfer Loss Measurements. - The shift-registers were fabricated on 1.0- and 30-ohm·cm p-type substrates with (100) orientation. The construction of these devices and the bonding are illustrated in Figs. 12 and 13. The operating circuit for these devices was similar

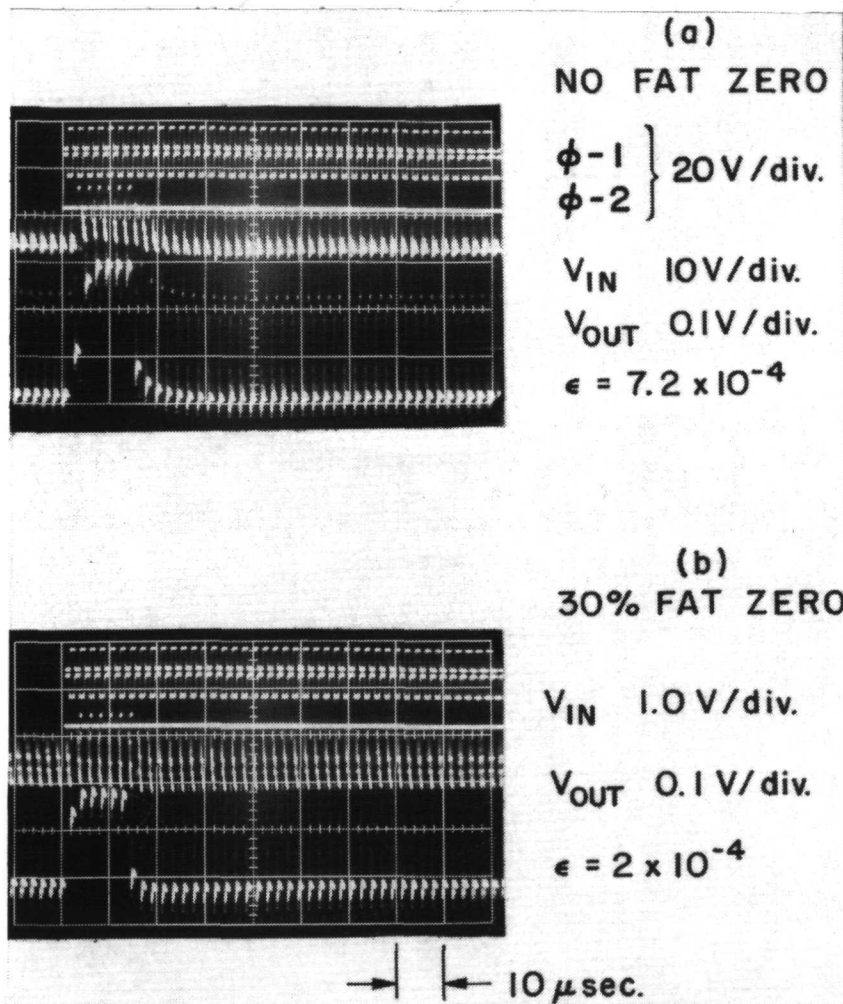


Figure 31. Waveforms for 1.0-mil-wide ( $25 \mu\text{m}$ ) 500-stage register at 250 kHz; 1.0-ohm·cm p-type substrate with (100) orientation.

to that shown in Fig. 14 except that separate dc bias voltages were provided for the polysilicon phase gates,  $E_{\phi}(\text{polysilicon})$  and for the aluminum phase gates,  $E_{\phi}(\text{aluminum})$  to simplify testing. The earlier setup had a dc substrate bias together with a dc offset between polysilicon gates and aluminum gates. The output stages for the 500-stage registers were also operated as inverter-amplifiers with the following dc bias voltages:  $V_{S-2} = 0$ ,  $V_{G-5} = +25$  V,  $V_{D-3} = V_{D-1} = +15$  V, and  $V_{G-4} = +10$  V.

The inverter-amplifier output was found to be satisfactory for clock frequencies from 5.0 to 10 MHz. For clock frequency of 10 MHz and above the experimental data were obtained by shunting the load device (D-2 to D-3) with a 1-kohm resistor.

Typical waveforms obtained in the operation of the 500-stage register are shown in Figs. 31 and 32. The waveforms in Fig. 31 are for a 1.0-mil-wide register made on 1.0-ohm·cm substrates. The dc bias voltages used

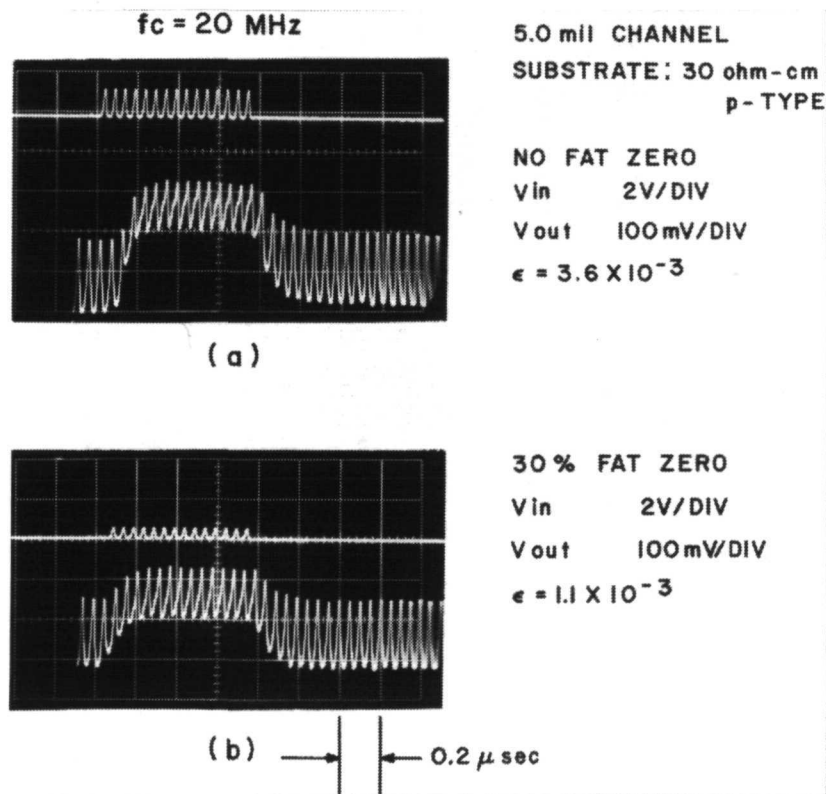


Figure 32. Waveforms for 5.0-mil-wide (125  $\mu\text{m}$ ) 500-stage register at 20 MHz; 30-ohm·cm p-type substrates with (100) orientation.

for the polysilicon and aluminum phase gates were  $E_{\phi}(\text{polysilicon}) = +10$  V and  $E_{\phi}(\text{aluminum}) = +5$  V. The measured transfer losses for 30% and 50% fat zero were  $2.0 \times 10^{-4}$  and  $1.4 \times 10^{-4}$ , respectively. This waveform was obtained during the probe testing of the devices on the wafer at a clock frequency of 250 kHz. The waveforms in Fig. 32 are for the 5.0-mil-wide register made on a 30-ohm·cm substrate. This device was operated with dc bias voltage applied to the polysilicon and aluminum phase gates  $E_{\phi}(\text{polysilicon}) = +5$  V and  $E_{\phi}(\text{aluminum}) = 0$ . The transfer loss per gate for this device operating with about 30% fat zero was measured as  $1.2 \times 10^{-3}$  at a clock frequency of 20 MHz.

2. Effect of the Polysilicon Field-Shield Bias Voltage. - In the operation of the 500-stage registers the polysilicon field shield was

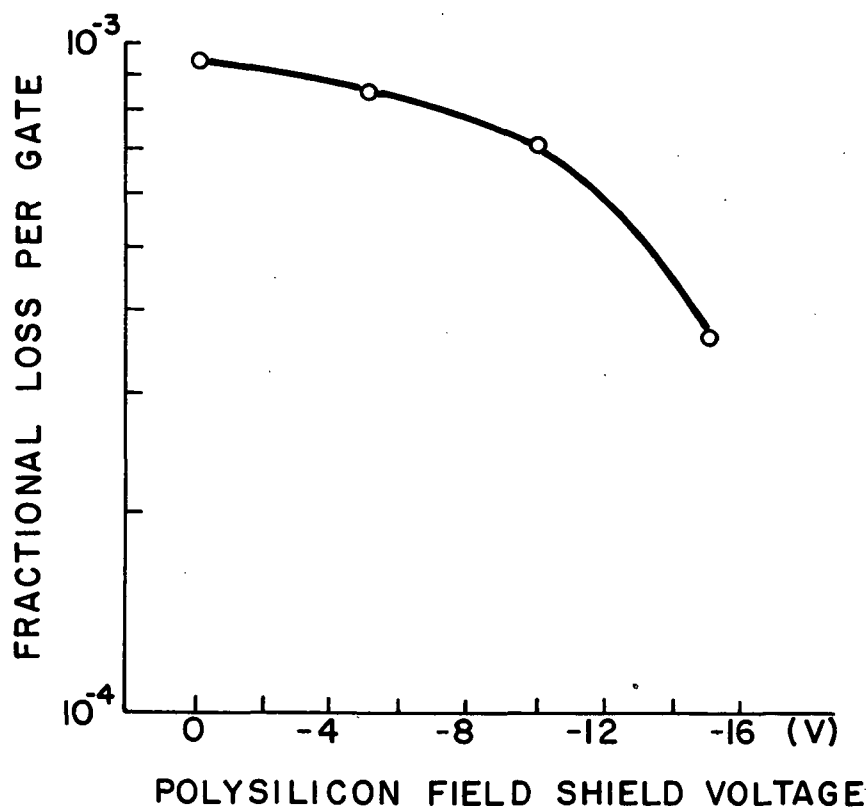


Figure 33. Effect of polysilicon field shield voltage on the transfer losses with no fat zero for 1.0-mil-wide ( $25 \mu\text{m}$ ) 500-stage register at 250 kHz; 1.0-ohm·cm p-type substrate with (100) orientation.

biased in the range of 0 to -15 V with respect to the substrate. The preliminary measurements made on the 1.0-mil-wide (25- $\mu$ m-wide) register with 1.0-ohm $\cdot$ cm substrate indicate that for operation with fat zero, the transfer losses change very little (if any) with the polysilicon field shield bias voltage,  $V_{F.S.}$ . For example, as the polysilicon field shield bias voltage was changed from 0 to -15 V, the transfer loss for 30% fat zero changed only from  $2.25 \times 10^{-4}$  to  $2.0 \times 10^{-4}$ . We have, however, observed a large change in the transfer losses for no-fat-zero operation with the variation of the polysilicon field shield bias voltage. This effect is shown in Fig. 33.

The fat-zero measurements of this device point out that the steepness of the edges of the CCD channel apparently is not appreciably affected by the bias voltage applied to the polysilicon field shield. The reduction in the transfer loss for no-fat-zero operation with the increase of the polysilicon field-shield voltage, shown in Fig. 33, is attributed to the increase in the thermally generated background charge which acts like a fat zero.

3. Transfer Loss Data. - The measured transfer losses for 1.0- and 5.0-mil-wide (25- and 125- $\mu$ m-wide) 500-stage two-phase registers made on 1.0- and 30-ohm $\cdot$ cm n-type substrates with (100) orientation are shown in Figs. 34 and 35. The fractional loss per gate for operation with about 30% fat zero is shown in Fig. 34. The data in Fig. 35 are for operation of these registers with no fat zero, or, in other words, without the constant circulating background charge required for reduction of the fast interface state losses.



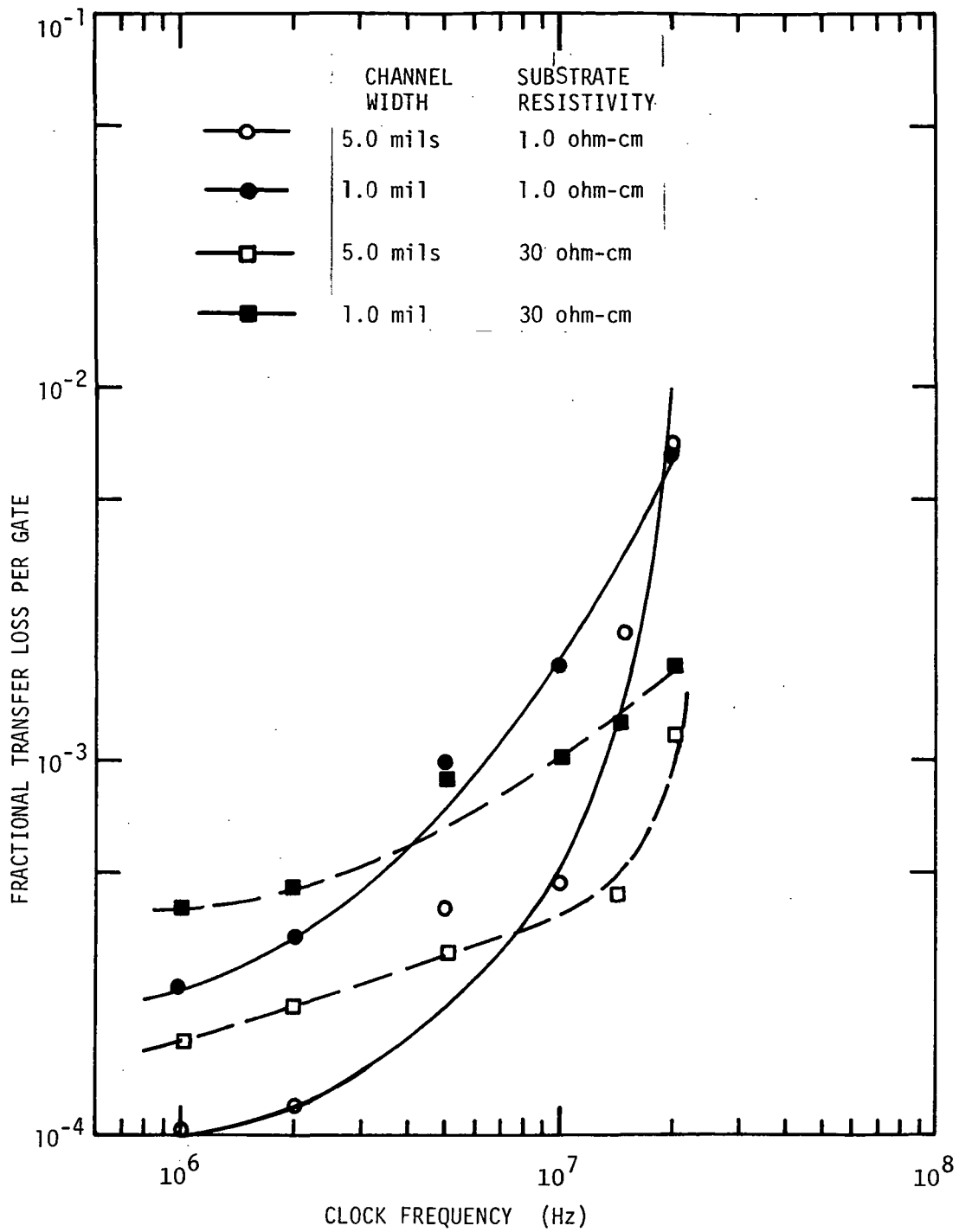


Figure 34. Transfer loss vs. clock frequency for 500-stage registers operating with 30% fat zero.

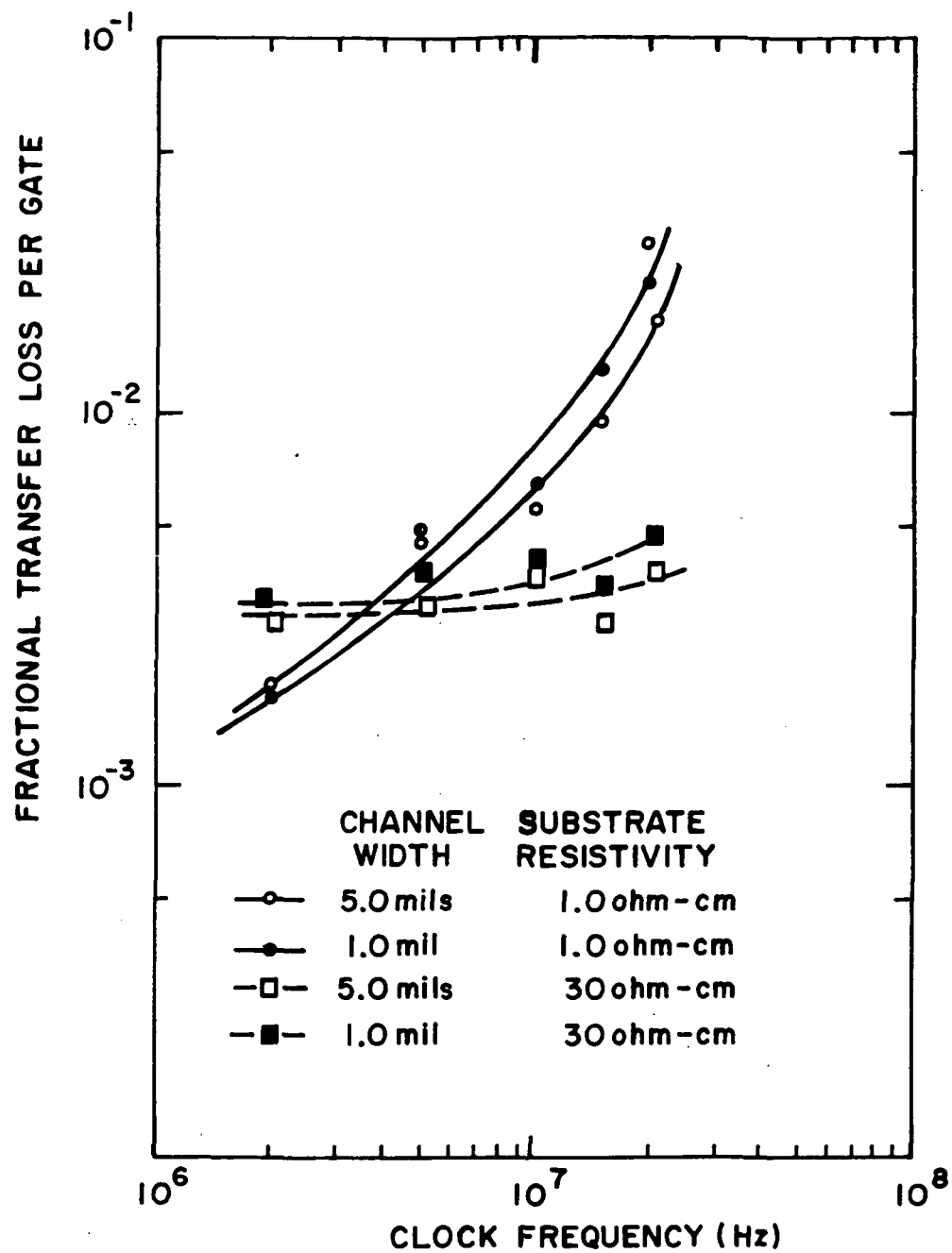


Figure 35. Transfer loss vs. clock frequency for 500-stage registers operating with no fat zero.

## V. DISCUSSION

### A. Correlation of Free-Charge-Transfer Analysis with Experimental Results

As discussed in Section II.A. of this report, the rate of charge transfer in a CCD may be appreciably increased due to the presence of drift-aiding fringing fields in devices with low substrate doping. The predicted performance of actual two-phase CCD's with polysilicon gate lengths of 10  $\mu\text{m}$  can be assessed by combining Eqs. (6) and (7), provided compensation is allowed for the difference between the three-phase structures which were assumed in the analysis and the two-phase structures studied experimentally. This is done by finding the 3-phase gate voltages required to achieve the surface potential actually found in the 2-phase device. For example, a two-phase polysilicon-aluminum structure with 1000-Å (0.1- $\mu\text{m}$ ) and 2400-Å (0.24- $\mu\text{m}$ ) oxide thicknesses,  $10^{16}$  doping, 5-V substrate bias, and 10-V pulses is equivalent with respect to surface potentials to a three-phase structure with 2 V on phase 1, 5 V on phase 2, and 9 V on phase 3, i.e., a 7-V pulse. Using a depletion depth under the transferring electrode appropriate for  $V = 5$ , we can calculate the frequency at which the fractional loss per transfer due to intrinsic free-charge-transfer limitation is  $10^{-3}$ , call it  $f_3$ . The time required to reach  $10^{-3}$  in the presence of fringing fields is approximately  $3\tau_t$ ; thus,

$$f_3 = \frac{1}{3(2\tau_t)} = \frac{1}{6\tau_t} \quad (19)$$

$$f_3 = \frac{1}{6} \frac{2\mu E_{\text{FMIN}}}{L} = \frac{13\mu x_{\text{ox}} V}{3L^3} \left[ \frac{5xd/L}{5 \frac{xd}{L} + 1} \right]^4 \quad (20)$$

This expression is plotted for both p- and n-channel devices in Fig. 36. The minimum frequency for both cases is set by thermal diffusion where

$$f_{3,\text{th}} = \frac{1}{8\tau_{\text{th}}} = \frac{2.5 (kT/q) \mu}{8L^2} \quad (21)$$

Also shown in Fig. 36 are experimentally observed points for four different 128-bit shift registers with differing resistivities and

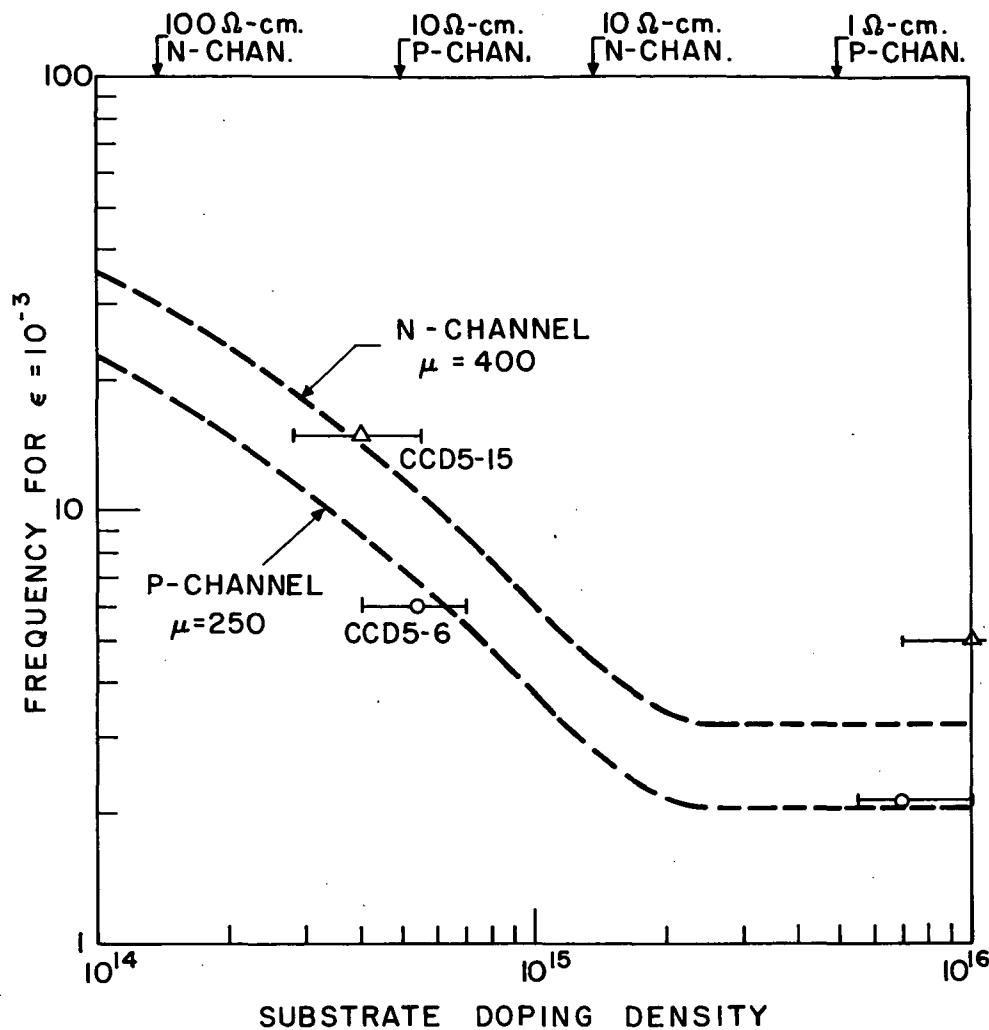


Figure 36. Frequency at  $\epsilon = 10^{-3}$  vs. substrate doping for both n- and p-channel devices with 10- $\mu$ m gate lengths.

channel types. Aside from the  $10^{16}$  doped n-channel, the agreement with the free-charge-transfer predictions is excellent.

The free-charge-transfer model also predicts an increase in speed as gate length decreases. In particular, for low-resistivity substrates in which fringing field drift should not be significant, the speed should increase as  $L^{-2}$ . The polysilicon gate length for the 64- and 128-stage devices is 10  $\mu$ m while the gate length for the 500-stage unit is 7.5  $\mu$ m. Hence, one would expect an increase of about 75% in the frequency where free-charge losses become significant. Figure 35 shows the fractional loss per transfer vs. frequency for the 500-stage devices without fat zero. The 1.0 ohm-cm unit with 5.0-mil-wide channel does not have a

well-defined frequency where the losses abruptly increase, but a corner frequency of 10 MHz is a reasonable choice, which is just twice the corner frequency of 1.0-ohm·cm devices with 10- $\mu$ m gate lengths (see Fig. 30).

The no-fat-zero results for 500-stage devices with 30-ohm·cm substrates in Fig. 35 are relatively flat but do seem to indicate the onset of increased losses. The with-fat-zero results shown in Fig. 34 seem to indicate a corner frequency between 20 and 30 MHz. (Experimental equipment limitations have so far prevented measurements above 20 MHz.) These results are in qualitative agreement with the theoretical predictions.

#### B. Correlation of Interface State Trapping Model Including the Edge Effect with Experimental Results

It has long been recognized that interface state losses would be an important factor in CCD operation, and such losses have been measured on both (100) and (111) substrates. The magnitudes of the losses are usually 5 to 10 times higher on (111) than on (100) substrates; this has been attributed to the higher interface state densities normally encountered on (111) substrates. Figures 27 and 28 show experimental measurements of interface state losses on 128-bit two-phase CCD's. In Fig. 27, curve B is for (111) substrates. The dotted line is a fit of the interface state model discussed in Section II. The fit indicates a fast-state density of  $1.2 \times 10^{11} \text{ (cm}^2 \cdot \text{eV)}^{-1}$ . In Fig. 28, curve C is for (100) substrates. Again, the dotted line is a model fit appropriate for  $N_{SS} = 2.9 \times 10^{10} \text{ (cm}^2 \cdot \text{eV)}^{-1}$ . (Note: The other curves in Figs. 27 and 28 do not apply to complete charge operation without fat zero and therefore do not reflect fast interface state loss.) It should be noted here that this type of measurement reflects the density of fast states approximately one-half the way between mid-gap and the minority-carrier band edge - in this case the valence band.

In order to independently measure fast-state densities on these devices, C-V and G-V measurements were made on devices similar to those shown in Figs. 27 and 28. The results are shown in Fig. 37. The G-V peaks are proportional to the fast-state density at mid-gap and correspond to values of  $4.6 \times 10^9 \text{ (cm}^2 \cdot \text{eV)}^{-1}$  for the (100) substrates and  $1.97 \times 10^{10} \text{ (cm}^2 \cdot \text{eV)}^{-1}$  for the (111) substrates. These values are somewhat lower than those predicted by the interface state model. This is probably due to the fact that the CCD technique measures states closer to the band edge, and the density of states is generally found to increase nearer the band edge. Probably the more significant factor to consider in evaluating the validity of the interface state model is the ratio of the densities for (111) and (100) substrates measured by

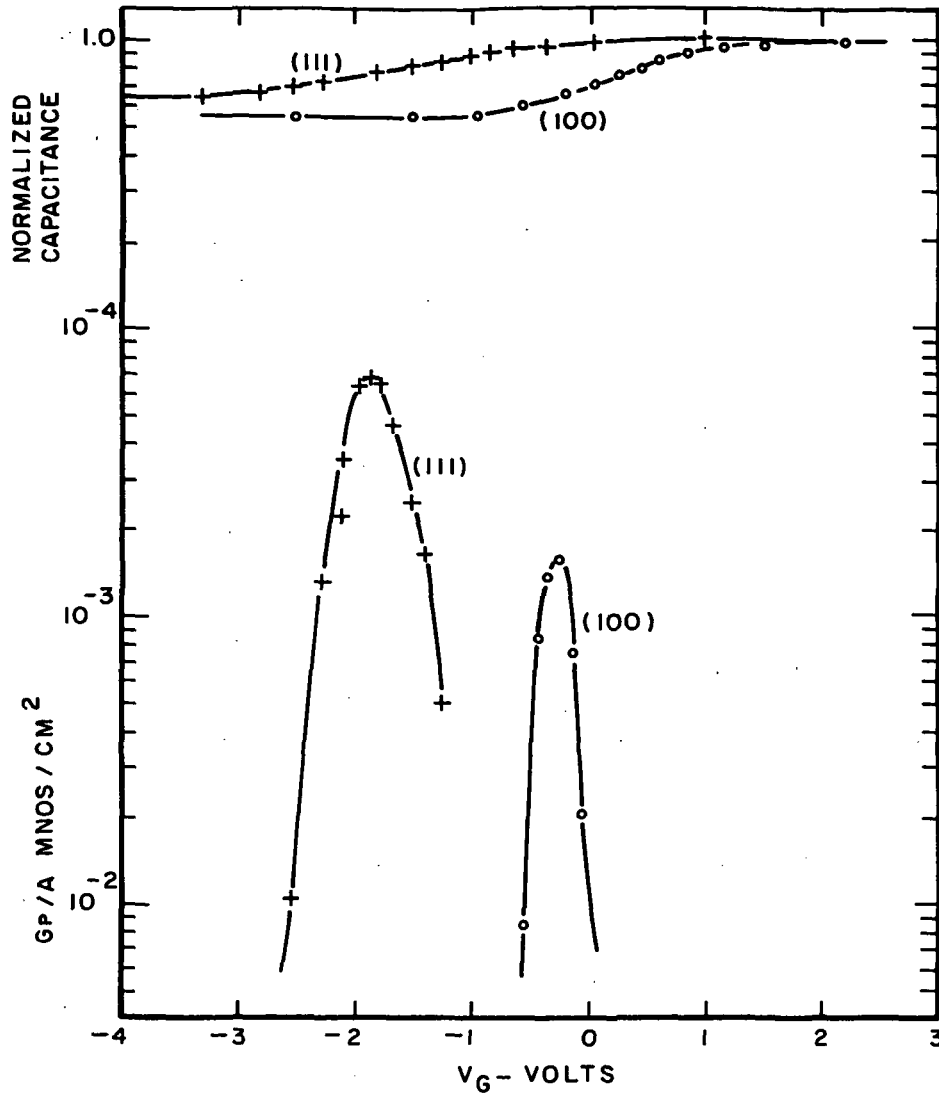


Figure 37. C-V and G-V measurements on (100) and (111) 128-stage CCD's.

CCD operation compared with the ratio obtained by G-V measurements. For CCD operation the ratio is  $12/2.9 = 4.1$ . The G-V ratio is  $19.7/4.6 = 4.3$ .

The degree to which fast-interface states influence transfer efficiency in the presence of fat zero is determined by the edge effect (see Section II.B.). Because of the rounded shape of the potential wells, a certain region near the edge cannot be exposed to fat zero and continues to cause losses even when fat zero is introduced. Thus, the

edge effect determines the maximum transfer efficiency that can be attained in surface-channel CCD's at moderate frequencies, i.e., those frequencies below the onset on significant free-charge losses.

As derived in Section II.B., the losses due to the edge effect should depend upon the channel width and the doping density, increasing for decreasing width and decreasing substrate doping. Since measurements have been made on devices with varying widths and doping densities, some preliminary correlation between theory and experiment is possible.

Figure 38 is a plot of transfer loss per gate versus channel width for several different substrate doping densities. The dotted lines indicate a fit of the theoretical predictions assuming a potential well depth of 4 V and a fast-state density of  $1 \times 10^{10} \text{ (cm}^2 \cdot \text{eV)}^{-1}$ . The data points for a given doping density follow the inverse dependence upon

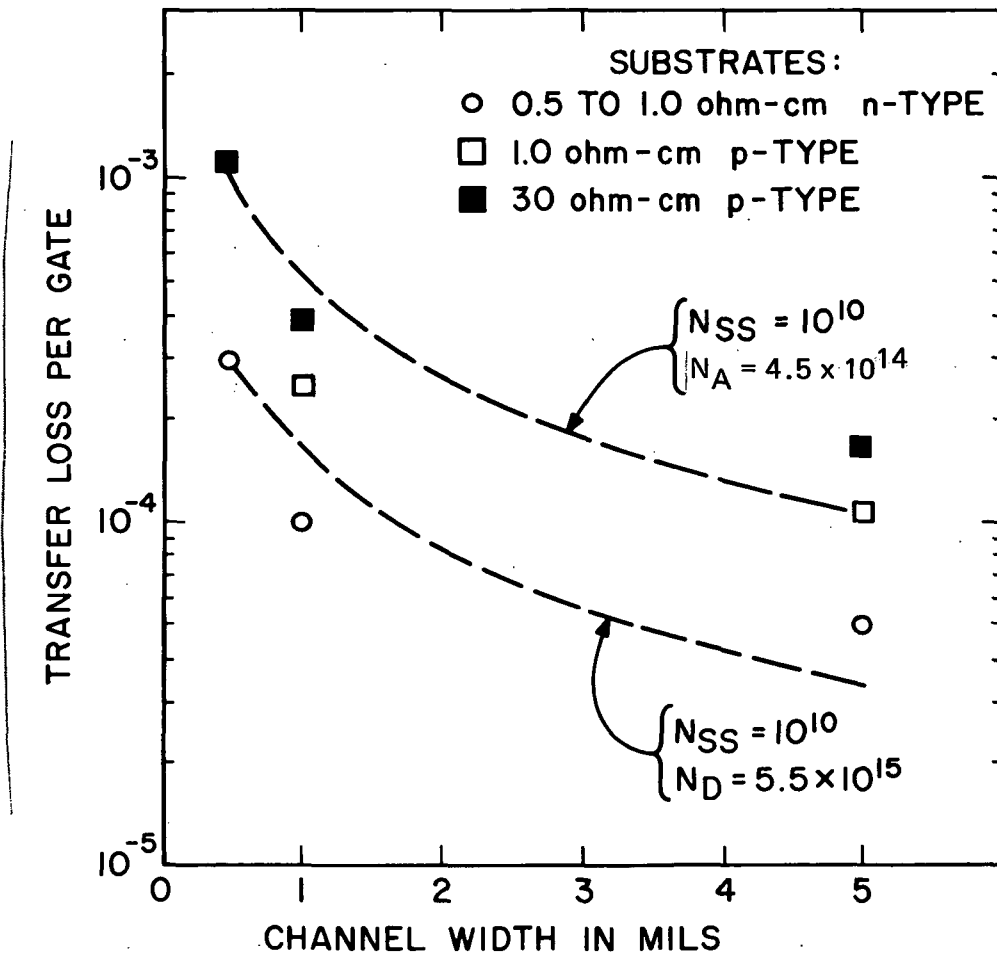


Figure 38. Experimentally measured fractional loss per gate vs. gate length. Dotted lines indicate theory.

channel width quite well, indicating our assumption that the edges of the potential wells perpendicular to charge flow (i.e., the "front" and "back") are relatively unimportant compared with the edges parallel to charge flow (i.e., the "sides"). In this case, then, the edge effect does not depend upon the length of the gate along the direction of transfer - only upon the width of the channel.

The dependence of the data upon doping density is also quite good, indicating that the simple one-dimensional model for determining the potential well slope is reasonable. As doping density decreases and the speed of free-charge transfer increases, the "rounding" of potential well increases and edge effect losses increase. Thus, one is trading lower losses at higher frequencies for higher losses at lower frequencies.

This speed efficiency trade-off depending upon substrate doping and channel width represents a very important design consideration for surface channel CCD's. The simultaneous achievement of speeds in excess of 15 MHz, channel widths of less than 1 mil (25  $\mu\text{m}$ ), and transfer efficiencies in excess of 99.9% (for gate lengths of 10  $\mu\text{m}$ ) appears to be unattainable for surface-channel CCD's with interface state densities greater than  $10^{10} \text{ (cm}^2\cdot\text{eV)}^{-1}$ . Therefore, shorter gate lengths and/or lower interface-state densities are required to exceed the above performance.

### C. Complete Charge (C-C) Transfer Mode Versus Bucket-Brigade (B-B) Mode

One very interesting feature of the two-phase CCD, which has separate external electrical access to both the polysilicon and aluminum gates, is that the device can be operated in a complete charge (C-C) transfer mode, or a bias-charge mode (ref. 16), also called the bucket-brigade (B-B) mode (refs. 17,18). This permits a convenient comparison of the limitations of CCD's vs. bucket brigades utilizing the same device. In the C-C mode, the "ON" aluminum gate produces a deeper surface potential than the "OFF" polysilicon gate so that all of the charge under the polysilicon gate can be transferred to the next stage. The magnitude of the surface potential is monotonically increasing as one moves from the "OFF" polysilicon gate to the "ON" polysilicon gate.

However, by changing the dc potential on the aluminum gates, one can shift to the B-B mode. Here the "ON" aluminum surface potential is shallower than the "OFF" polysilicon surface potential so that a potential barrier exists that tends to keep a portion of the charge trapped behind, under the "OFF" polysilicon gate. We have called this mode the bucket-brigade mode because the operation of the device is similar to the operation of the bucket-brigade device (refs. 17, 18).



The "OFF" polysilicon gate with free charge trapped behind the potential well formed by the "ON" aluminum acts like a source diffusion, and the potential barrier under the "ON" aluminum acts like the channel in the bucket-brigade device. The charge transfer terminates in the same subthreshold field-effect transistor (FET) current flow that characterizes the bucket-brigade device.

Our initial two-phase CCD's were made on 1.0-ohm·cm n-type substrates with (111) orientation. Most of these devices operated in the B-B mode or near the transition between the C-C and B-B mode. To operate these devices in the C-C mode, a larger dc bias had to be applied to the aluminum gates than to the polysilicon gates. To ensure operation in the C-C mode with a wide range of substrate-bias voltages, the devices for which most experimental data are presented were made with a channel-oxide thickness under the aluminum gates of 2400 Å (0.24 μm) and using 1.0-ohm·cm substrates n-type with (100) orientation. These devices operated in the C-C mode for phase bias voltages ranging from 1 V to about 18 or 20 V. Therefore, rather large substrate-bias voltages had to be used to obtain the B-B mode of operation. To minimize the effect of the dark current in the comparison of the transfer losses between the C-C and B-B modes for operation with no fat zero, measurements were made on a device with low and uniform dark current. The B-B mode of operation was also obtained by applying a larger dc bias voltage to the polysilicon gates than to the aluminum gates.

A more quantitative illustration of the biases required for operation of the registers in the C-C and B-B modes is given in Figs. 39 and 40. The surface potential curves for the polysilicon and aluminum gates were computed for substrate doping of  $10^{16}$  cm<sup>-3</sup> and the flat-band voltages were adjusted to conform with the measured threshold voltages for the devices made on substrates with (100) orientation, i.e.,  $V_{th}(\text{polysilicon}) = -0.6$  V and  $V_{th}(\text{aluminum}) = -3$  V. The C-C mode with dc bias  $E_{\phi} = -5$  V and clock-voltage swing of  $\Delta\phi = 10$  V is shown in Figs. 39 and 41 (b). In this case,  $\Delta\phi_3$  corresponds to the maximum signal that can be transferred when the device is operated with overlapping pulses. With nonoverlapping clock pulses, the maximum transferable signal corresponds to  $\Delta\phi_1$ .

The operation of a two-phase register in the B-B mode is shown in Figs. 40 and 41(c). Here, the transition to the B-B mode was accomplished by maintaining the aluminum gates at a dc bias voltage  $E_{\phi} = -5$  V, while the dc bias voltage applied to the polysilicon gates is increased to  $E_{\phi} + E = 15$  V. As a result of this new biasing condition, a barrier potential,  $\Delta\phi_2$ , shown in Fig. 41(c), is formed under the aluminum transfer gate. Because of this potential barrier, during the continuous operation of the register in the B-B mode, a conductive layer is maintained under the polysilicon gates that operationally resembles the diffusions of a bucket-brigade structure.

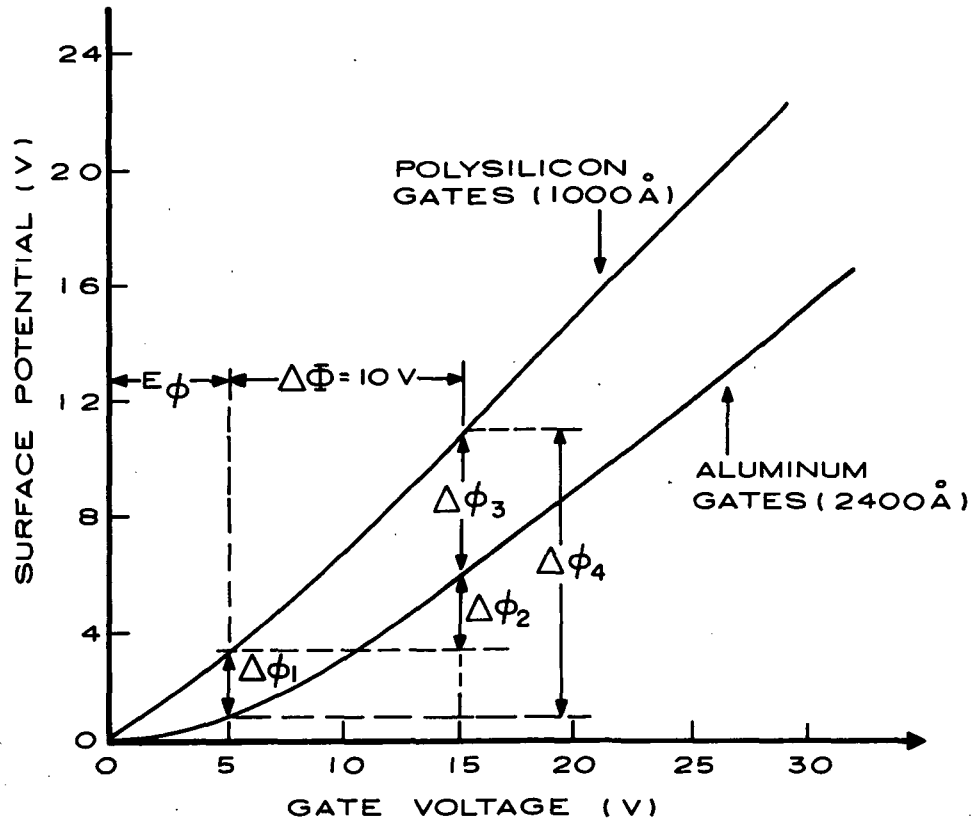


Figure 39. Calculated surface potentials versus gate voltage for polysilicon gates and aluminum gates having channel oxide of 1000 Å (0.1  $\mu$ m) and 2400 Å (0.24  $\mu$ m), respectively, and substrate doping  $N_D = 10^{16} \text{ cm}^{-3}$ . Complete charge-transfer mode is obtained for both gates with the same dc bias of 5 V and phase voltage swing of 10 V ( $E_\phi = 5$  V,  $E = 0$ , and  $\Delta\phi_1 = \Delta\phi_2 = 10$  V).

The transition from the C-C mode to the B-B mode can also be made by increasing the substrate bias or phase bias  $E_\phi$ . No dc potential difference between polysilicon and aluminum gates is required. This is illustrated in Fig. 40. The requirement for B-B mode is that the 'ON' aluminum has a smaller surface potential than the 'OFF' polysilicon. The crossover point is obtained by shifting the aluminum-gate surface potential by the clock voltage  $\Delta\phi = 10$  V, as shown by the dotted surface potential curve in Fig. 40. The gate voltage where this dotted and shifted aluminum curve intersects the unshifted ('OFF') polysilicon curve is the dc phase bias above which the B-B mode should apply and below which the C-C mode should apply. The calculated value

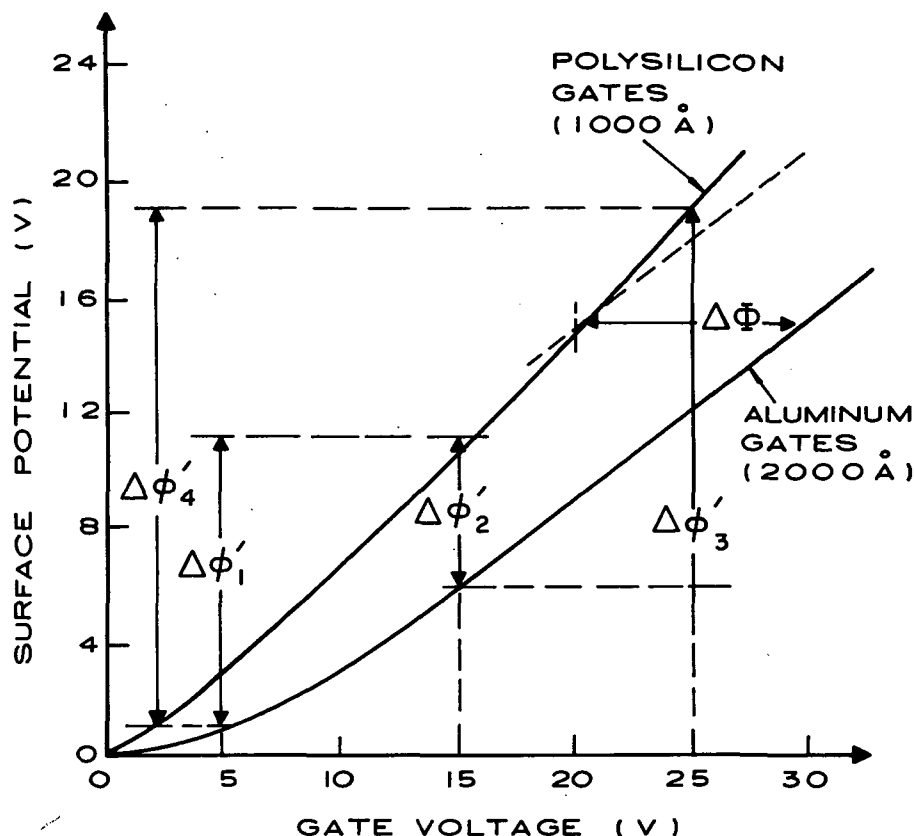


Figure 40. Bucket-brigade mode of operation is illustrated for polysilicon gates biased with 15 V and aluminum gates with 5 V ( $E_\phi = 5$  V,  $E = 10$  V, and  $\Delta\phi-1 = \Delta\phi-2 = 10$  V).

of this crossover bias voltage (approximately 20 V) is in reasonably good agreement with the experimentally observed values of 18 to 20 V.

Another good agreement between the experimental data and the calculated operation shown in Figs. 39 through 41 is the detected output voltage swing,  $\Delta V_{out}$ . According to the calculations in Figs. 39 and 41(b), full well signal charge should correspond to a surface-potential charge,  $\Delta\phi_3 \cong 5$  V. The value is consistent with the maximum detected output signal,  $\Delta V_{out} = 1.5$  to 2 V, taking into account the total capacitance associated with the output diffusion,  $C_F \approx 1.2$  pF, and the total capacitance of the storage gate,  $C_{ox} + C_D = 0.4$  pF.

Finally, the difference in the expected charge-transfer characteristics between the C-C mode and the B-B mode is illustrated in Fig. 42. As shown in Fig. 42(a), the final transfer of charge in the

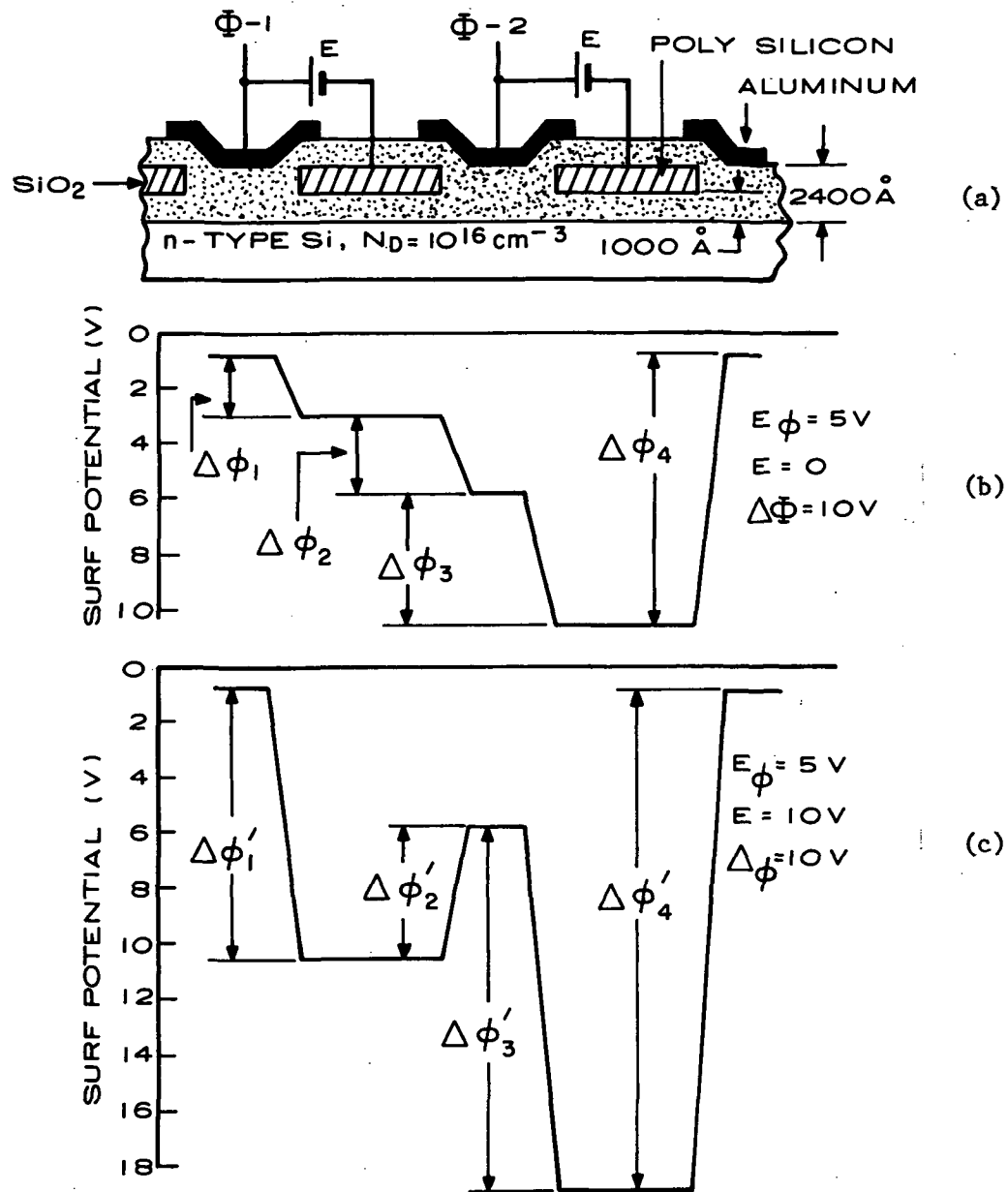
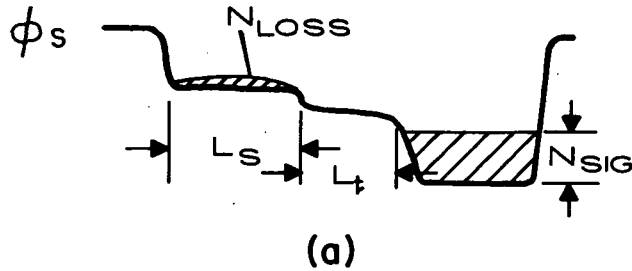


Figure 41. (a) Surface potential profiles for two-phase charge-coupled structure, (b) operating in the C-C mode, and (c) in the B-B mode.

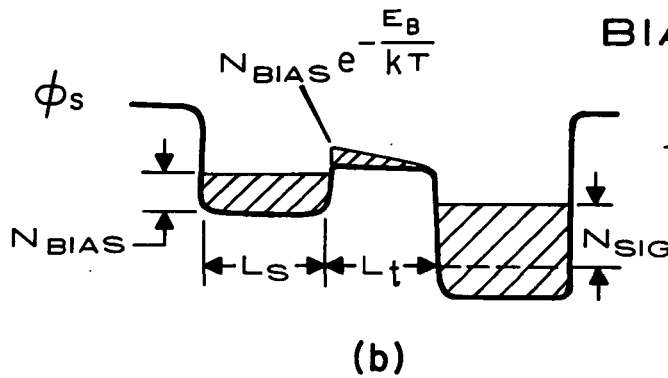
## COMPLETE CHARGE TRANSFER



$$\frac{N_{LOSS}}{N_{SIG}} = e^{-\frac{t}{\tau}}$$

$$\tau_{TH. DIFF} = \frac{L_s^2}{2.5D}$$

$$\tau_{FR. DRIFT} = \frac{1}{3} t_{transit}$$



## BIAS - CHARGE MODE

$$\tau_B = \frac{L_s L_t e^{-\frac{E_B}{kT}}}{D}$$

Figure 42. Comparison of the charge-transfer characteristics (a) for the C-C mode and (b) for the B-B mode.

C-C mode is expected (ref. 7) to take place either under the influence of thermal diffusion with a time constant

$$\tau_{th Diff} = \frac{L_s^2}{2.5D} \quad (22)$$

where D is the diffusion coefficient, or, when applicable, by fringing-field (ref. 8) drift with estimated time constant

$$\tau_{FR Drift} = \frac{1}{3} t_{transit} \quad (23)$$

Here,  $t_{\text{transit}}$  represents the transit time of a single carrier in the fringing field.

In the case of operation of two-phase CCD's in the B-B mode, the initial-charge-transfer process is expected to be similar to the C-C mode except that the critical length is the transfer gate  $L_t$ . But because of the presence of the potential barrier under the transfer gate, the final transfer of charge is expected to involve injection of the charge across the barrier as illustrated in Fig. 42(b).

After the charge in the first well is reduced below the barrier under the transfer gate, thermal diffusion will continue with time constant  $\tau_B$

$$\tau_B = \frac{L_S L_t}{D} \exp\left(\frac{E_B}{kT}\right) \quad (24)$$

where  $E_B$  represents the difference between the quasi-Fermi level for  $N_{\text{BIAS}}$  and the flat-barrier voltage under the transfer gate. The expression for  $\tau_B$  assumes no fringing field under the transfer gate.\*

An interesting effect was observed concerning the fractional loss per gate as a function of frequency for devices operating in the B-B mode with a small barrier voltage (see curves A and B in Fig. 29). For operation with fat zero, curve A, the transfer loss continued to decrease as the clock frequency was reduced. On the other hand, without fat zero (curve B), a sharp decrease in the transfer loss was observed as the clock frequency was reduced below 100 kHz.

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\*The experimental demonstration of the C-C and B-B modes of operation of two-phase CCD's and the proposed model illustrated in Fig. 42(b) were originally described by the authors at the 1972 ISSCC in Philadelphia.

## VI. CONCLUSIONS

The development of two-phase charge-coupled devices in the form of polysilicon gates overlapped by aluminum gates (ref. 6) has been continued by fabricating and testing 64-, 128-, and 500-stage registers. The devices studied included a variety of 0.5-, 1.0-, and 5.0-mil-wide (12.5-, 25-, and 125- $\mu\text{m}$ -wide) two-phase registers with p- and n-channels made on low- and high-resistivity substrates. The method of channel confinement employed included thick-field oxide, diffusion guard rings, and polysilicon field shield.

The best overall performance has been achieved with 5-mil-wide (125- $\mu\text{m}$ ) n-channel devices made on substrates with (100) orientation. For operation at clock frequencies of 1.0 MHz and below, the devices made on 1.0-ohm $\cdot\text{cm}$  substrates were operated with a charge-transfer loss of less than  $10^{-4}$  per transfer; and devices made on 30-ohm $\cdot\text{cm}$  substrates exhibited a transfer loss of  $10^{-3}$  at clock frequencies of 20 MHz.

The experimental results were found to be consistent with the free-charge transfer theory (ref. 7), predicting increased speed as the substrate doping and gate length decreases. An additional speed performance trade-off due to rounding off the potential walls, i.e., the so-called edge effect, has been experimentally demonstrated. The edge effect loss becomes more pronounced in devices with narrower channels and in devices made with lower substrate doping. On the basis of experimental data, an edge-effect loss model was developed that predicts that the simultaneous achievement of speeds in excess of 15 MHz, channel width of less than 1.0 mil (25  $\mu\text{m}$ ), and transfer efficiencies greater than 99.9% (for gate lengths of 10  $\mu\text{m}$ ) is unattainable for surface channel charge-coupled devices with interface-state densities greater than  $10^{10}(\text{cm}^2\text{-eV})^{-1}$ . Therefore, shorter gate lengths and/or lower interface state densities are required to exceed the above performance.

The fast interface state densities estimated from the experimental work for p-channel devices made on 1.0-ohm $\cdot\text{cm}$  substrates were  $1.2 \times 10^{11}$  and  $2.9 \times 10^{10}(\text{cm}^2\text{-eV})^{-1}$  for substrate orientations of (111) and (100), respectively.

A comparison of the complete charge-transfer mode (C-C mode) and the bias-charge or bucket-brigade mode (B-B mode) of operation of the registers showed that at 1.0-MHz clock frequency the complete charge-transfer mode is greater than 10 times more efficient than the bias charge mode. At higher clock frequencies, such as 10 MHz, the two modes of operation were found to have about the same charge-transfer efficiency. Both of these results were obtained with fat-zero operation. For operation without fat zero, the charge-trapping-like transfer losses for the B-B mode were found to be larger than for the C-C mode. This effect was clearly demonstrated in registers made on (100) substrates.

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